Three Presentations: Corporate, MIPS P5600, MIPS M5100 / M5150

March 2014

www.imgtec.com

Corporate Overview

December 2013

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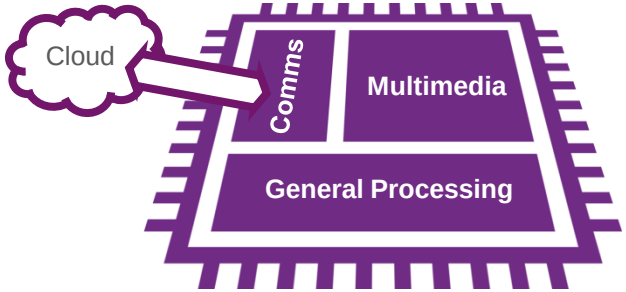
Company overview

- **Leading silicon, software & cloud IP supplier**
  - Multimedia, processors, communications, cloud
  - Licensing & royalties based business model
- **Targeting high volume, high growth markets**
  - Semiconductor manufacturers and OEMs
  - Mobile, home consumer, automotive, storage, networking, infrastructure, IoT
- **Pure: our strategic product division**
  - Digital radio, connected audio, home automation
- **Established technology powerhouse**
  - Founded 1985; London FTSE 250 (IMG.L)
  - UK HQ; global operations with ~1,600 employees



Imagination

Comprehensive IP portfolio for SoCs & cloud connectivity

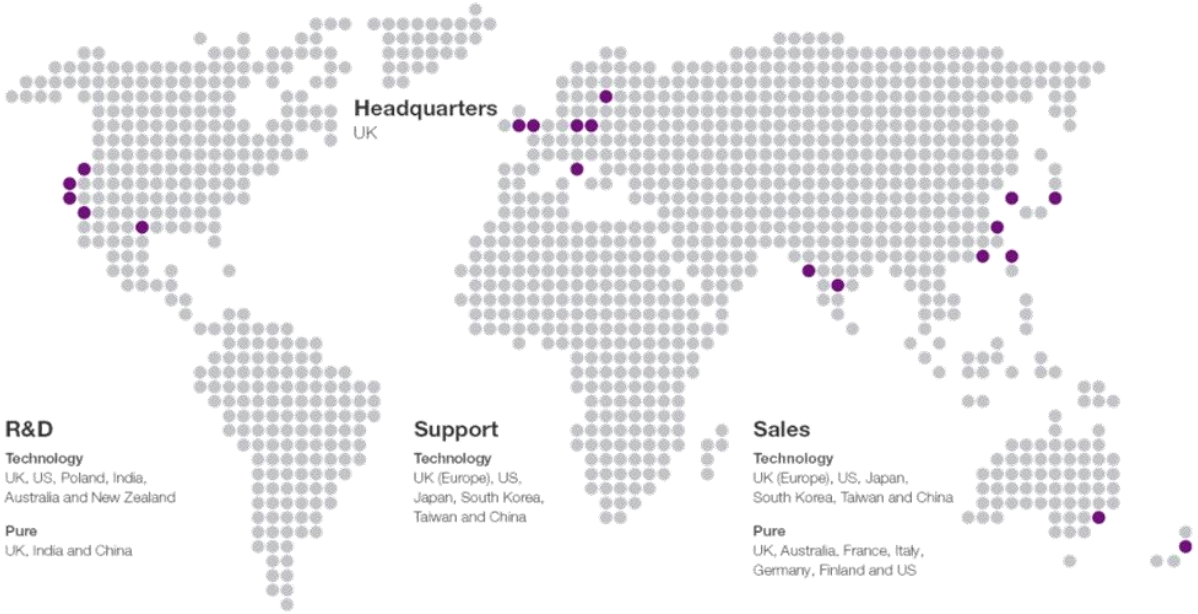
PURE

IP business pathfinder
Market maker/driver

Imagination is global

Growing R&D, support and sales world-wide

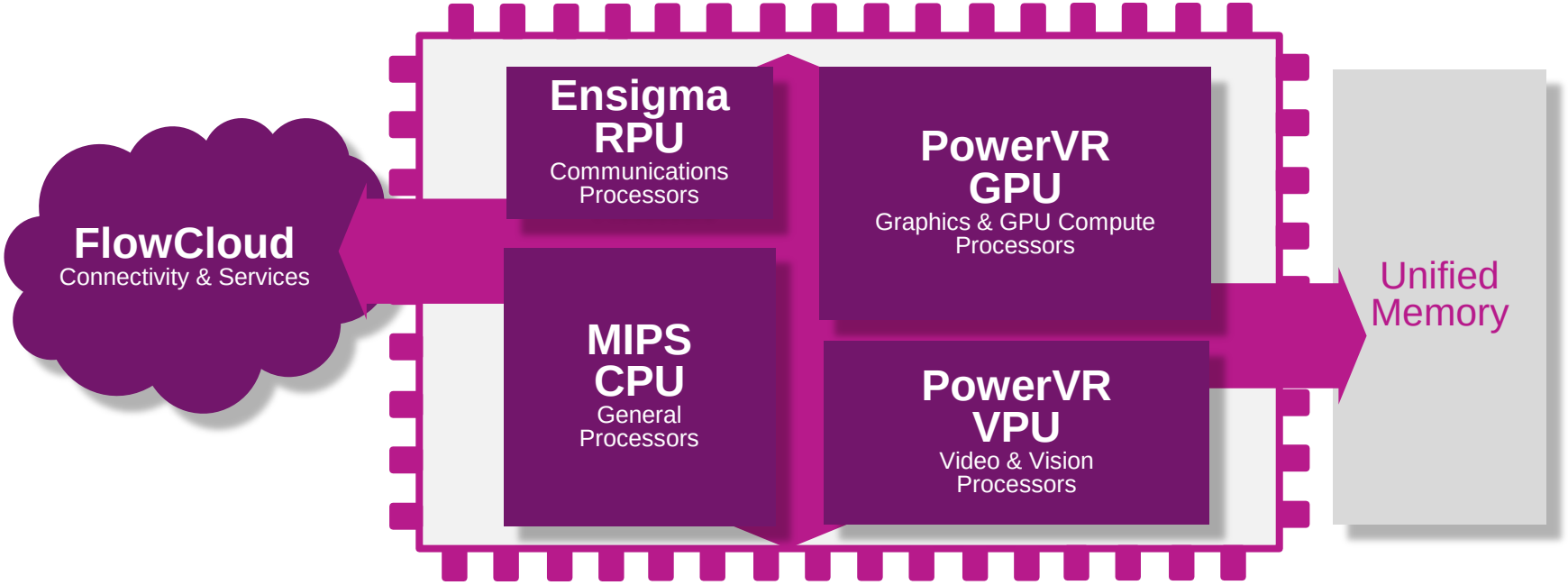
- **UK: global HQ**
  - 4 R&D centres
- **USA: a major focus**
  - >250 people
  - 6 US offices
  - R&D, support, sales
- **India: key R&D centre**
  - 3 offices
- **Asia: sales & support**
  - across every major country



Our operations reflect both our customers' needs and global engineering centres of excellence

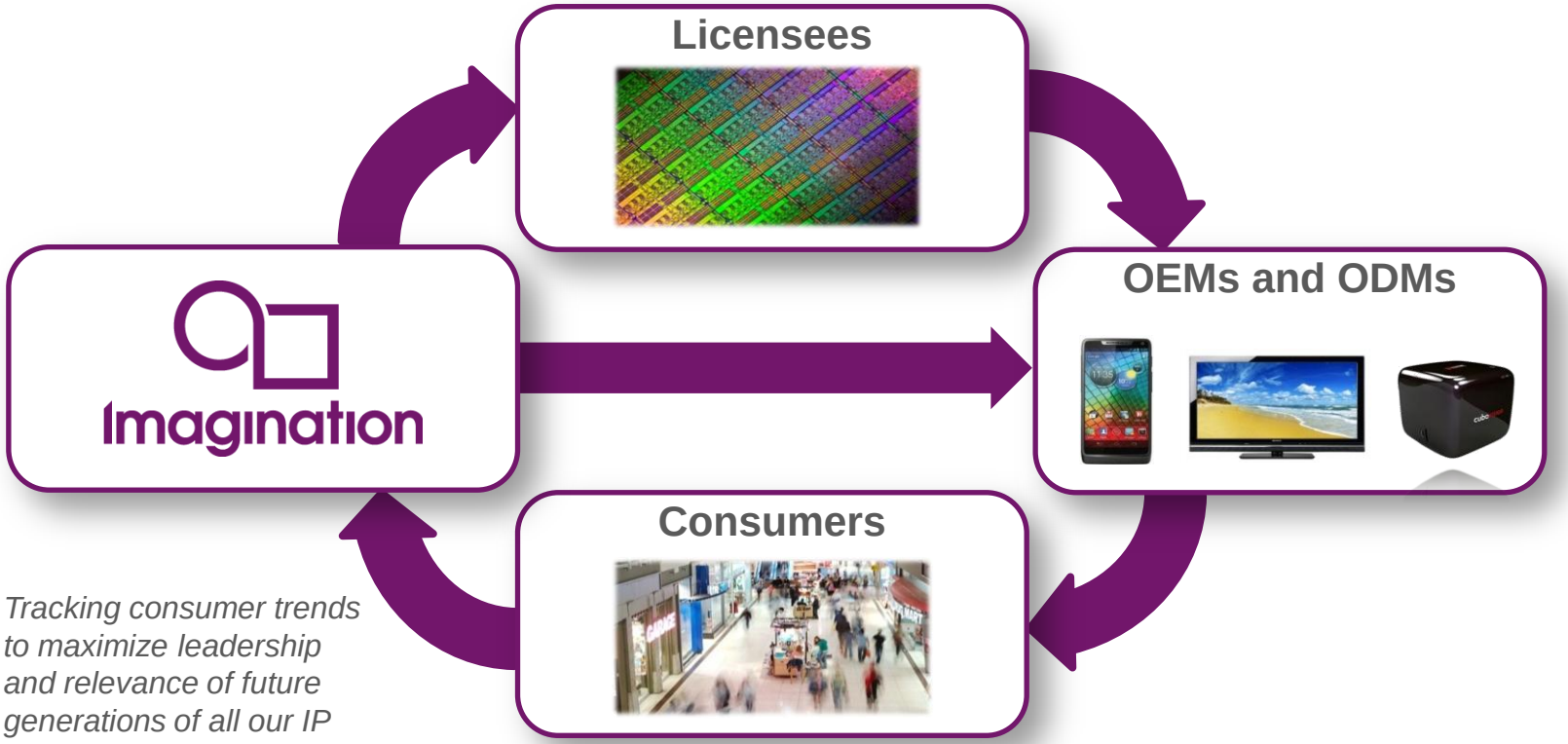
Imagination's IP portfolio

Everything needed to create connected SoC solutions



All of Imagination's IP stand as class leaders in their field, and also work together to create unrivalled solutions for our increasingly connected, media-rich world

Business model



Tracking consumer trends to maximize leadership and relevance of future generations of all our IP

Diversifying licensees

Globally, across all markets, from high end to low end

Strategic partnerships are key

Close relationships with key industry partners ensures our technology leadership

In more products than ever before

Note: now includes MIPS

Megatrends

- **Moore's Law slowing down - but it doesn't matter**
- **Open source redefining software investment and possibilities**
- **The speed and reach of internet opening up new business models**
- **Products are getting more human-centric**
  - MS-DOS reached 1% of the world's population; smartphones will reach 50%
  - IoT in health, energy, security etc will touch everyone and everything
- **Supply chains creating more routes to market**
  - Return to vertical integration - in many forms : "Vertical 2.0"
  - Differentiation for brands is a key motivation
  - More opportunities developing for solution-centric technologies
- **Platform approach addresses complexity and ecosystem**

Delivering subsystems and platforms is key to respond to these trends

Imagination is driving emerging markets

- Our IP is already in major emerging applications markets
- We have the fundamental IP to build any kind of device

Product Overview

What we do

An unrivalled silicon & software IP portfolio for SoCs

Multimedia

PowerVR GPU: Graphics, Compute

PowerVR RTU: **R**ay Tracing

PowerVR VPU: Video & Vision

Processors

MIPS CPU: Performance & Embedded

OS: Android, Linux, RTOS, …

Tools: GNU, LLVM, Debug, Probes

Communications

Ensigma RPU: connectivity

Ensigma RPU: broadcast receivers

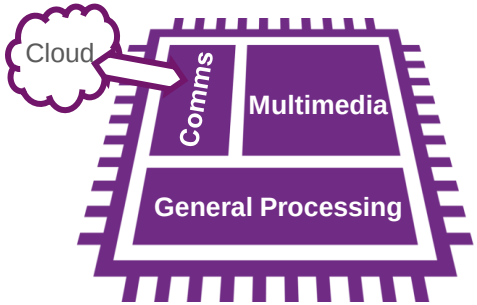
HelloSoft: V.VoIP & VoLTE

Cloud

FlowCloud: Server & Client Technology

FlowCloud: Comprehensive APIs

FlowCloud: Growing ecosystem, IoT, M2M



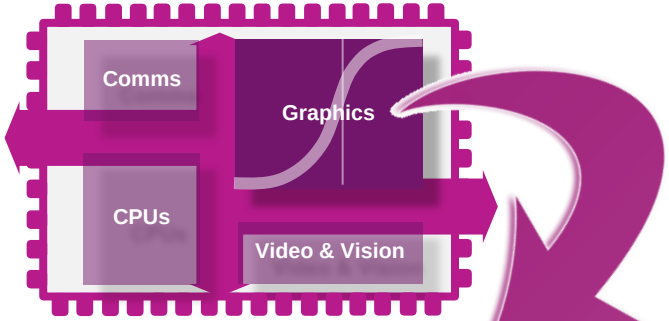
Complementary businesses – supporting new technologies

PURE 

VISUALIZER 

PowerVR: the established GPU leader

Unrivalled graphics; GPU compute delivers exceptional performance



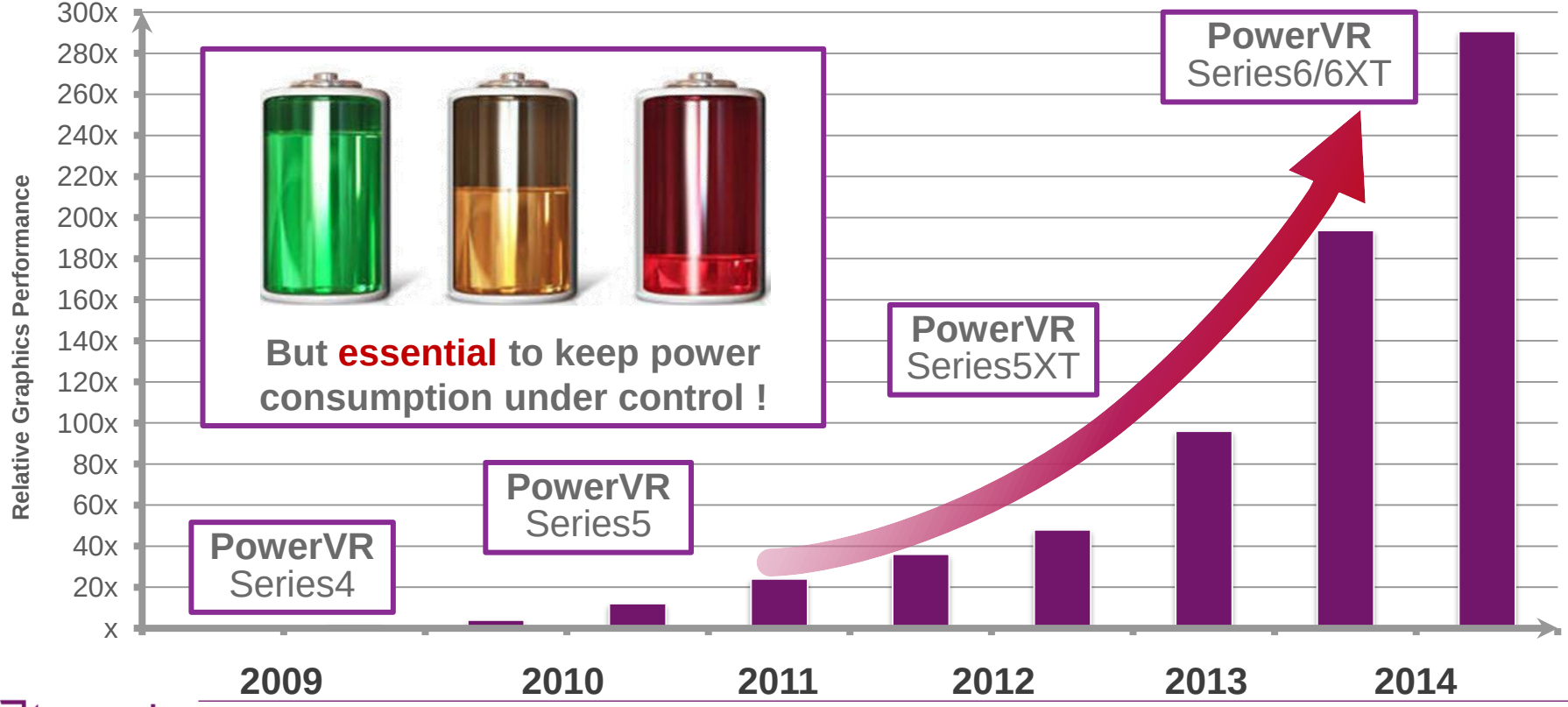
- **Industry's leading power efficiency**
- **Industry's leading area efficiency**
- **Unrivalled performance under real operating conditions thanks to TBDR***
- **Latest Series6XT moves performance efficiency to a new level**

* TBDR: Tile Based Deferred Rendering

PowerVR GPUs set the benchmark for mobile graphics & GPU compute

Mobile GPUs now 200x the first smartphones

Whilst keeping the overall power consumption low

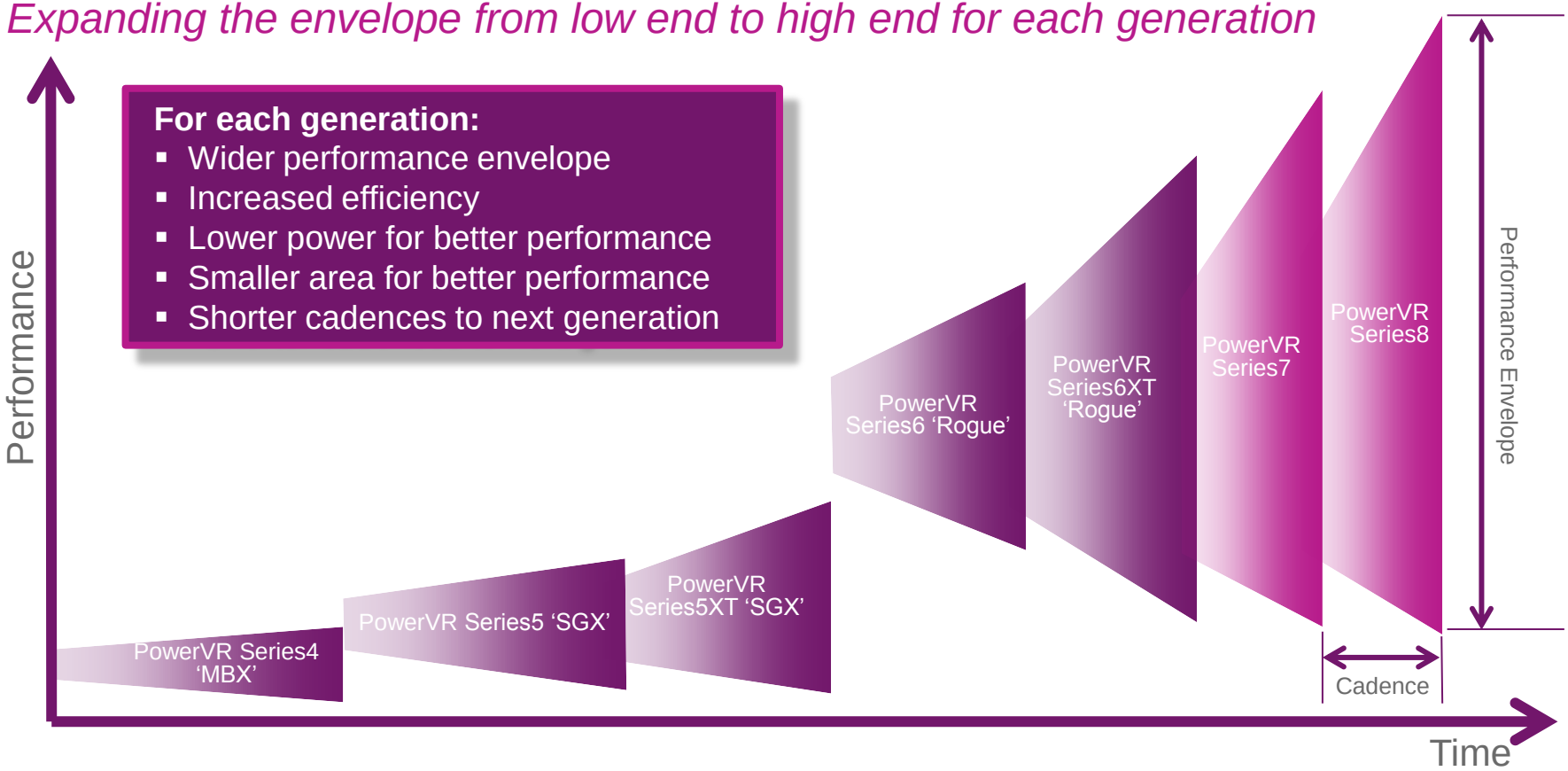


Keeping PowerVR GPUs ahead of the pack

Expanding the envelope from low end to high end for each generation

For each generation:

- Wider performance envelope
- Increased efficiency
- Lower power for better performance
- Smaller area for better performance
- Shorter cadences to next generation

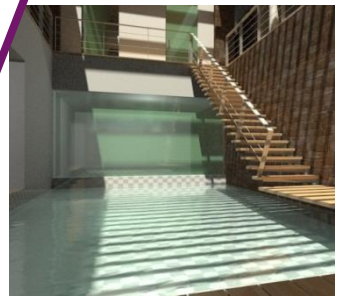


Innovation in GPUs: Ray Tracing

The behaviour of light is not inherently supported in conventional graphics

- Current graphics use ‘pre-baked’ lighting to emulate reflections, shadows etc
- Never looks realistic
- Not dynamic, so limits freedom of content creation

- Hardware Ray Tracing Unit (RTU) models light inherently, so every scene delivers rich image realism
- Content creation is much simpler



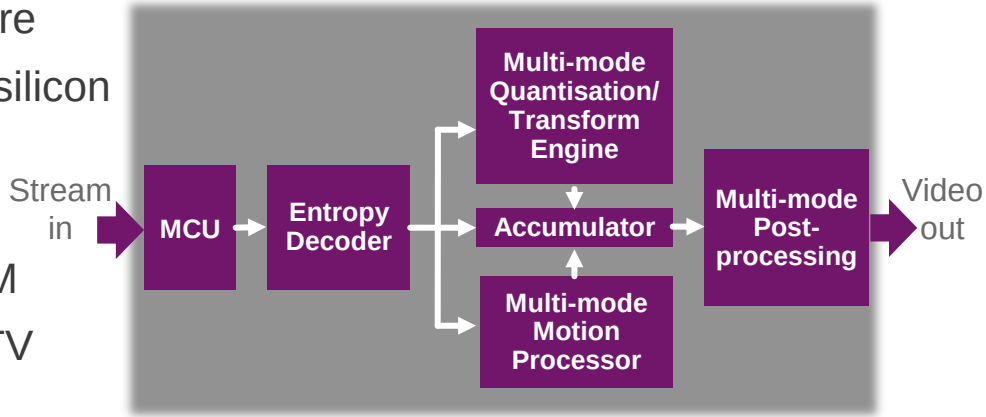
PowerVR Ray Tracing is uniquely efficient and will be disruptive

VPU video: efficiency at blazing speeds

- **Video >70% network traffic & going 4K!**
  - Compression with no compromise is essential
  - HEVC & H.265 essential to cope with future demand
- **Standards very well defined and stable**
  - Fully optimised using configurable hardware
  - Fully programmable video engines waste silicon and power for mainstream applications

PowerVR Series4 VPU

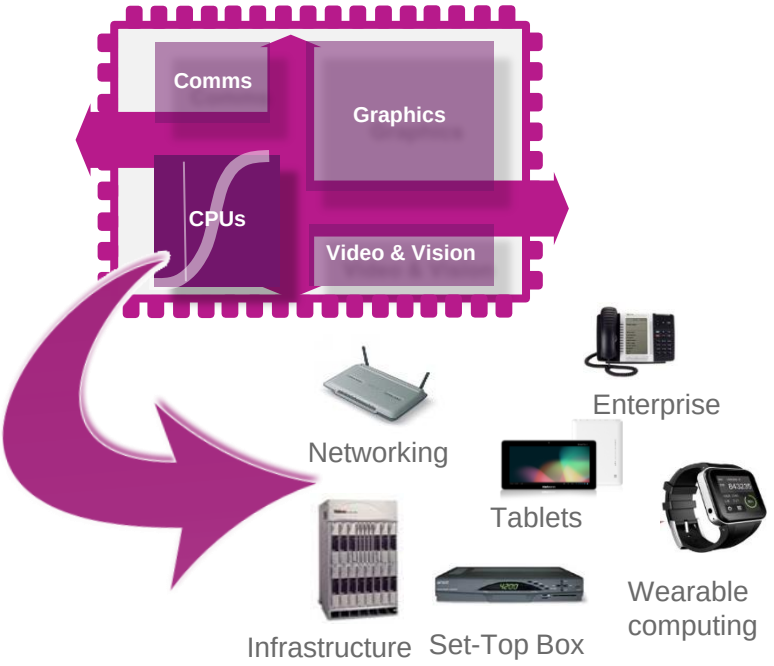
- <10mW for 1080p60 HD decode in 28HPM
- Full support for 10-bit colour, 4K for UHDTV
- Full support for 4:4:4, 4:2:2



Video processor architectures need optimised hardware, flexibility and high compression for encode

MIPS: changing the game

Powering the connected SoC



- **World's most mature 64/32 bit architecture**
- **MIPS Series5 Warrior CPU core portfolio:**
  - M class: ultimate embedded
  - I class: ultimate power/performance
  - P class: ultimate performance
- **Industry leading PPA* across the range**
- **Area up to 40% less than competitors**
- **Unique multi-threading for multi-core**
- **Strengthening Android, Linux, RTOS support**

* PPA: Power, Performance, Area

Changing the CPU landscape from low to high end – welcomed by industry

MIPS: changing the game

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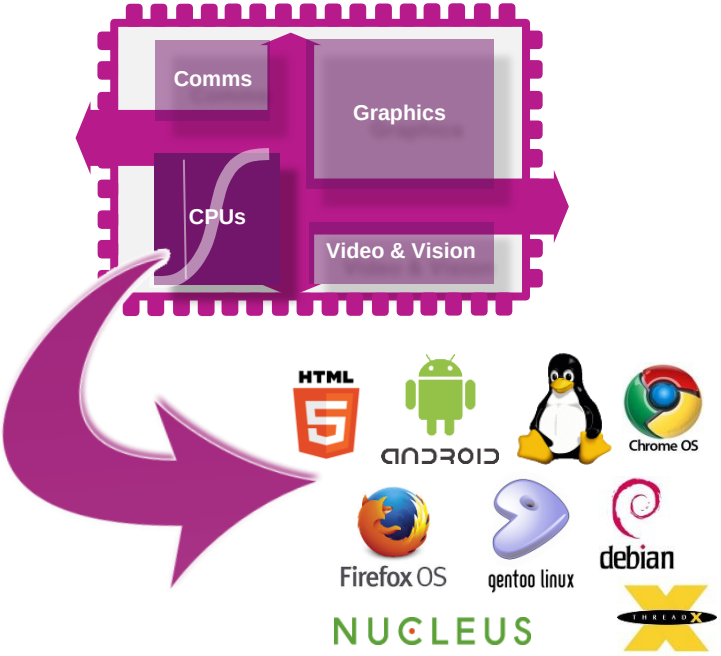

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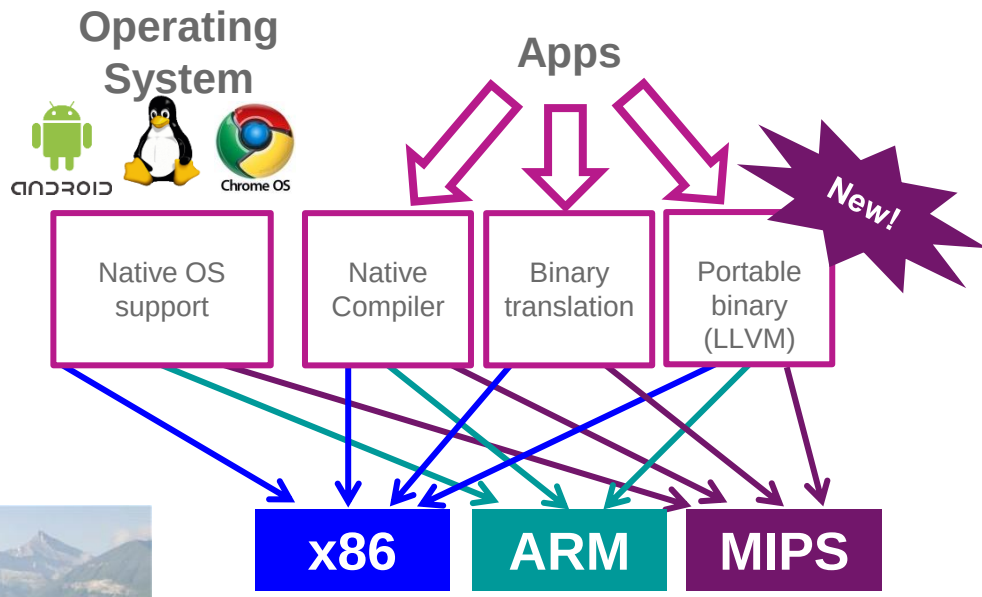
From closed to open

NOKIA

symbian

Only approved ARM-based chips

The old days: Restricted hardware platform; high cost for OS per phone; dominated by Nokia



SoC Platform CPUs

The new era: ISA dependence is coming to an end..

CPUs: everywhere and growing

Every product has many CPUs and MCUs

Smart Phone:
5-10 CPUs

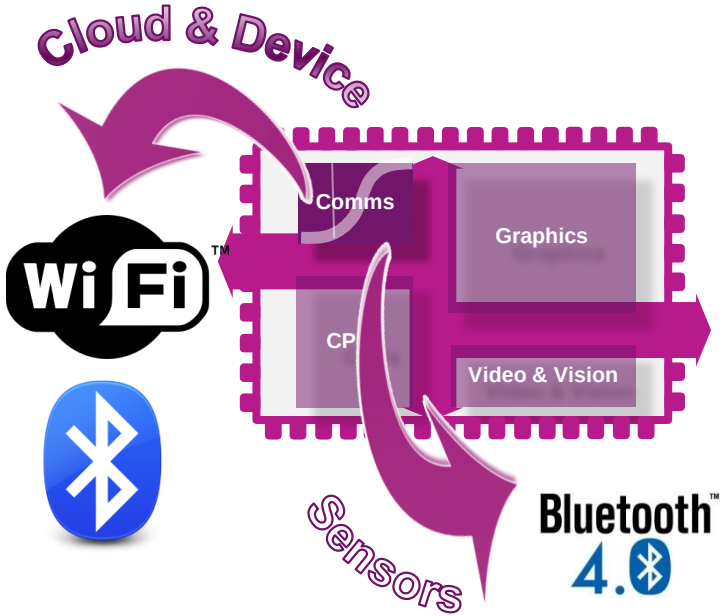
Smart Car:
30-50 CPUs

Smart House:
100s of CPUs

CPUs are everywhere – it's an enormous and growing IP market

Ensigma comms: the next wave

The most efficient multi-standard on-chip communications solution available



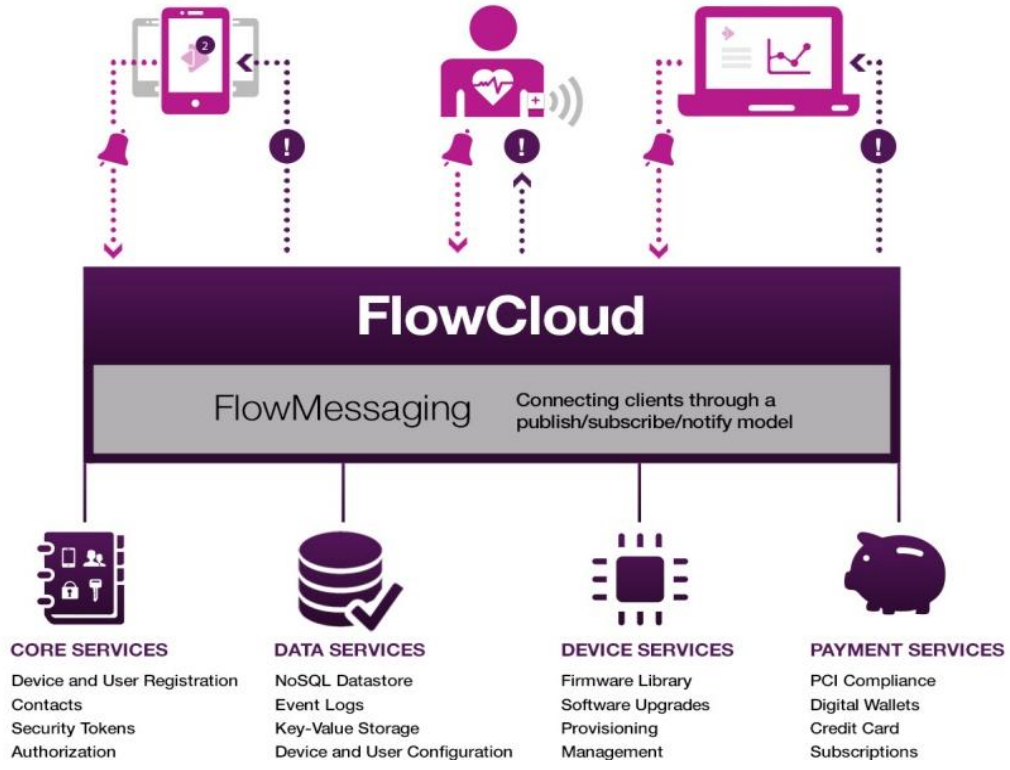
- **Wi-Fi solutions to 802.11ac gaining traction**
  - Wi-Fi/BT/FM combo IP just announced
- **Multi-standard TV gaining market share**
- **Scalable technology**
  - New ultra low-power interfaces
  - Ideal for IoT sensors

Connected SoCs are the future
The Ensigma RPU is the ideal scalable and proven answer

Making the Internet of Things reality

Our technologies power devices – and the best way to connect them

FlowCloud
by Imagination



- Well-defined APIs
- Basic services "shrink-wrapped"
- Device to Cloud
- Device to Device
- Subscription & transaction-based business model
- Optional value-added services
  - Music, radio, VoIP

Flow powered Apps

The digital home revolution is coming

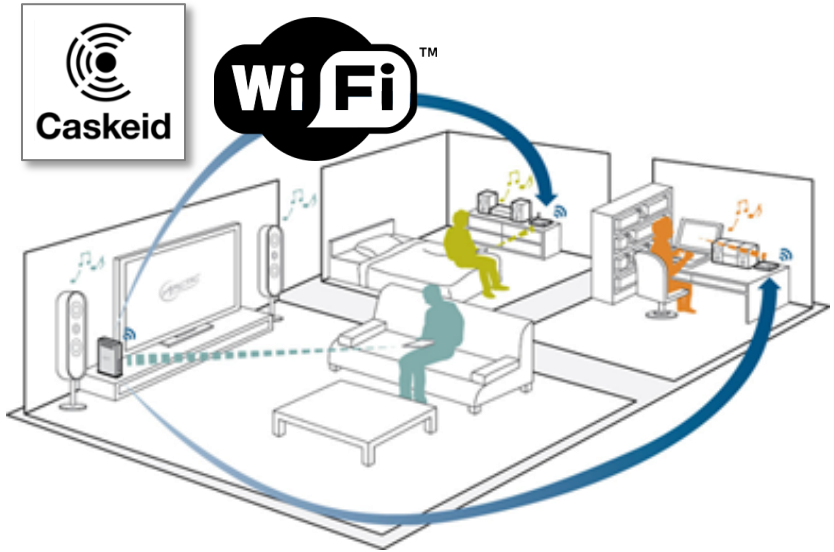
Everything going wireless – but will they work together?

- **Consumers expect their content everywhere**
  - Streamed from the cloud and locally
  - controlled by smartphones & tablets
- **Everything must work together**
  - Multimedia, home automation, security, eHealth must all join up
- **Imagination delivers system level IP to help make this a reality**
  - FlowCloud: hardware + software infrastructure & services
  - FlowAudio: music and radio
  - FlowTalk: V.VoIP telephony
  - Caskeid®: high performance, ultra low latency multiroom audio streaming

Wireless audio as good as wired: Caskeid®

Example of technologies developed by Pure

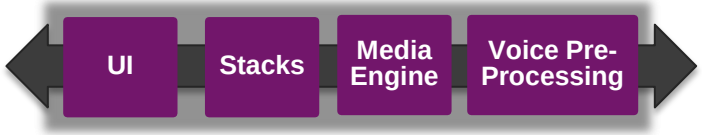
- **Patented technology to precisely synchronize audio streams over Wi-Fi**
- **Uses industry standard Wi-Fi (802.11)**
- **Wireless speaker solutions built around SoCs using Imagination's Ensigma and FlowCloud connectivity IP**
- **Perfectly synchronised multiple speakers**
  - …as many as you like!
- **Fully integrated with FlowAudio**
- **Available for licensing now**

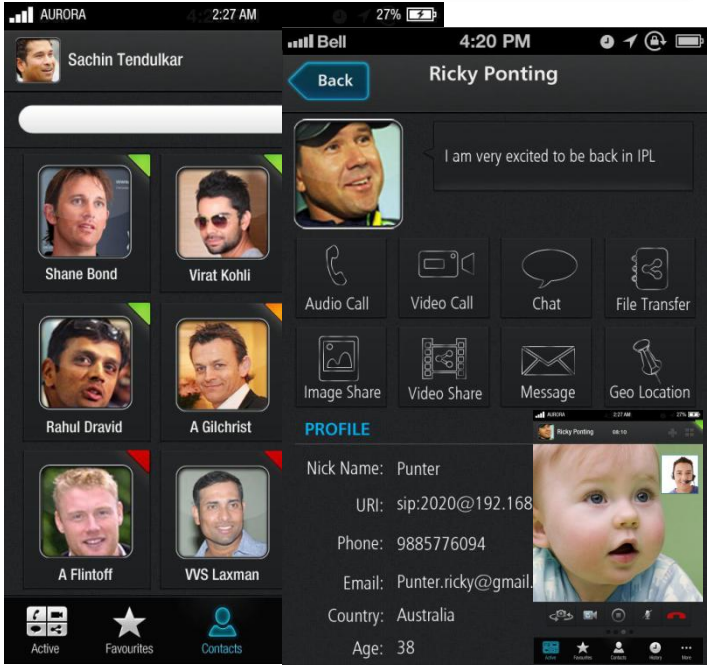


Enabling rich video &voice over IP

VoLTE, V.VoIP & RCS software delivers ultimate solution

HelloSoft by Imagination





- **Integrated and unified solution**
  - Includes voice, video and rich communications
  - EVQM (Enhanced Voice Quality Management)
  - DVQM (Dynamic Video Quality Management)
- **Common stack and optimized media engine**
- **Any platform**
  - Android, iOS, Linux, Windows, RTOS
- **Multiple access networks**
  - Wi-Fi, 3G, 4G/LTE, 10/100 Ethernet
- **Any mobile or consumer device**
  - Smartphones, tablets, PCs, TVs, STBs, CPE, cars
- **Any processor**
  - MIPS, x86, ARM, other DSPs and CPUs

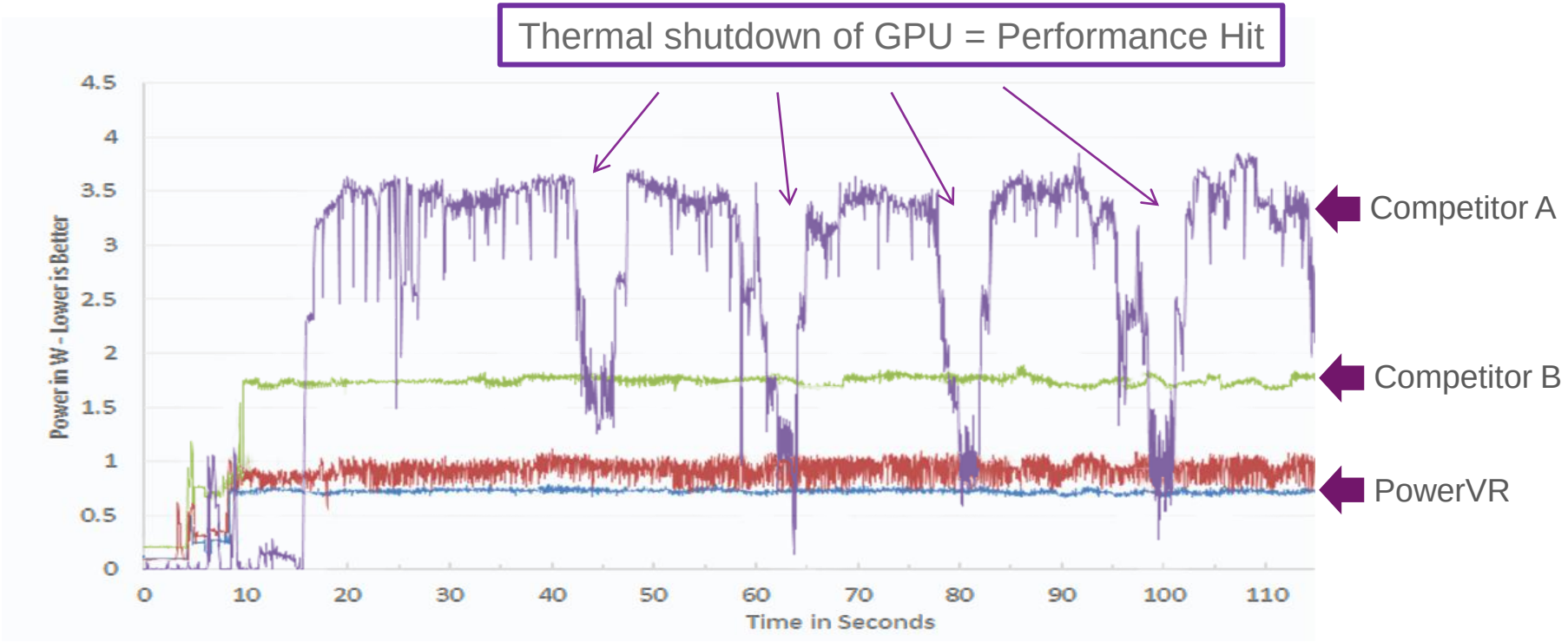
Power: the ultimate battleground

Already dominates 28nm design; will define sub 20nm SoCs

- **Power will increasingly dominate every major design decision for SoCs**
  - Not just for mobile
- **Thermal envelope is vital for mobile products**
- **Benchmarking usually ignores power**
  - Sustained performance in a real system is what matters
  - Imagination's call to action for benchmark vendors
- **'Dark silicon' (part of silicon powered up only for peak demand) and advanced power management strategies will be key product differentiators**

GPU power efficiency and thermal impact

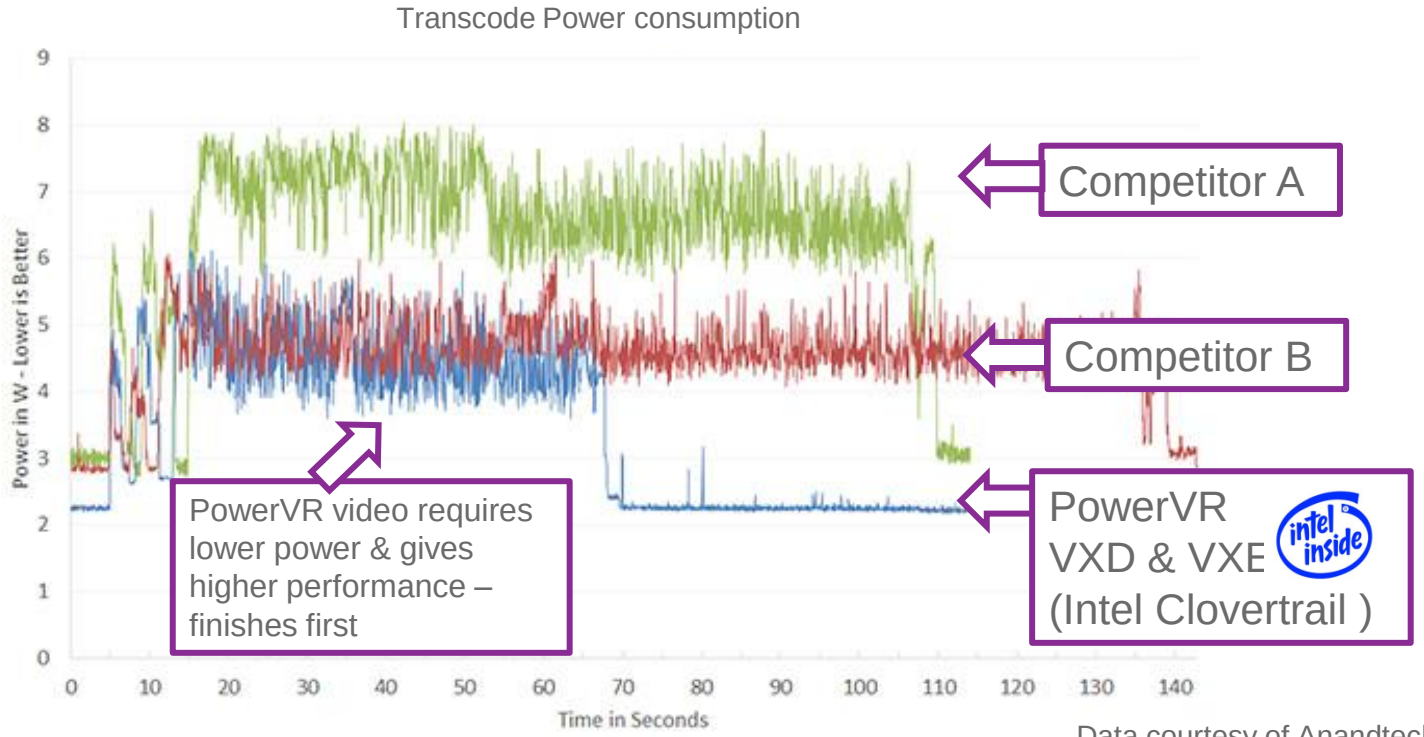
High power consumption = heat = risk of thermal panic = reduced performance



Data courtesy of Anandtech.com

Video power consumption

Transcode example

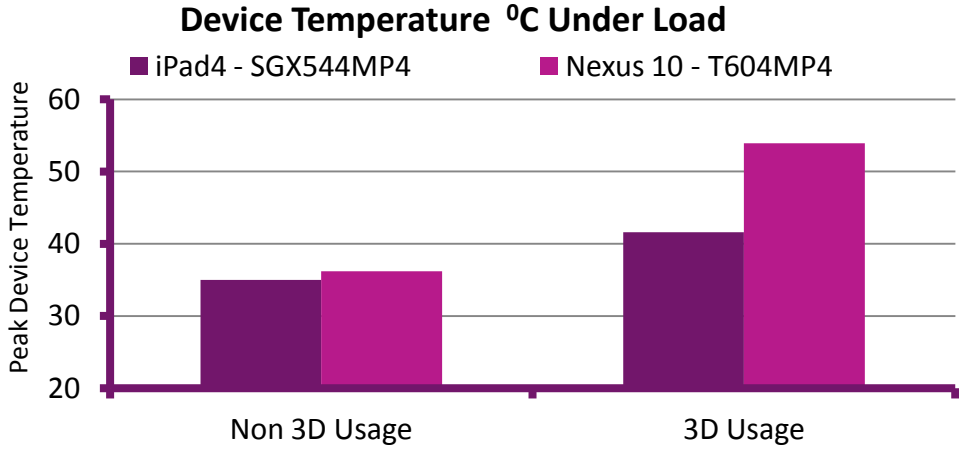


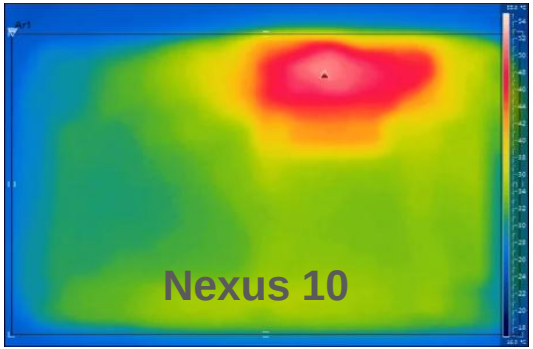
Data courtesy of Anandtech.com

PowerVR power consumption leads competition

SGX and Rogue Efficiency focussed architectures

- **3rd Party measured data from http://www.playwares.com/xe/25745383 (Korea)**
  - Temperature is directly linked to power consumption of the device
    - note iPad4 is also delivers 50% more Graphics performance – Energy/FPS Impact
  - Shows that iPad4 running **GLBenchmark 2.5 Egypt HD** runs much “cooler” than Nexus10
    - confirms lower power consumption & higher efficiency of PowerVR solutions





Thermal image of SoC under load

Imagination

PURE

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Pure drives market segments

…that matter to Imagination's IP business

- **Digital Radio – job mostly done**
  - Digital switchover, global penetration underway
  - Before: DAB digital radios were £500
  - Pure entered market with £99 radio…
    - Now you can buy DAB for £20

  Imagination powers over 80% of the growing DAB market

- **Connected Home Audio – today's focus**
  - The next home electronics revolution, driven by smart devices & streaming technologies
  - Migration from high-end fragmented market to mainstream consumer imminent
  - Pure paving the way
- **Connected Home - future**
  - More connected devices and automation coming - IoT

New products driving strategy

- **Products driving digital radio**
  - Consumer and automotive

- **Products driving connected audio**
  - Products, apps, services
    - Music services live in UK, US, France

- **Strategic engagements**
  - Significant interest from and engagements with key players developing around our audio platform

Jongo multiroom wireless speakers

PURE

Unique patented low latency audio distribution over Wi-Fi

- **Jongo allows you to add as many speakers in as many rooms as you like**
- **With Bluetooth you can stream music to one speaker at a time**
- **With Wi-Fi go multiroom and seamlessly play your music through multiple speakers in multiple rooms**

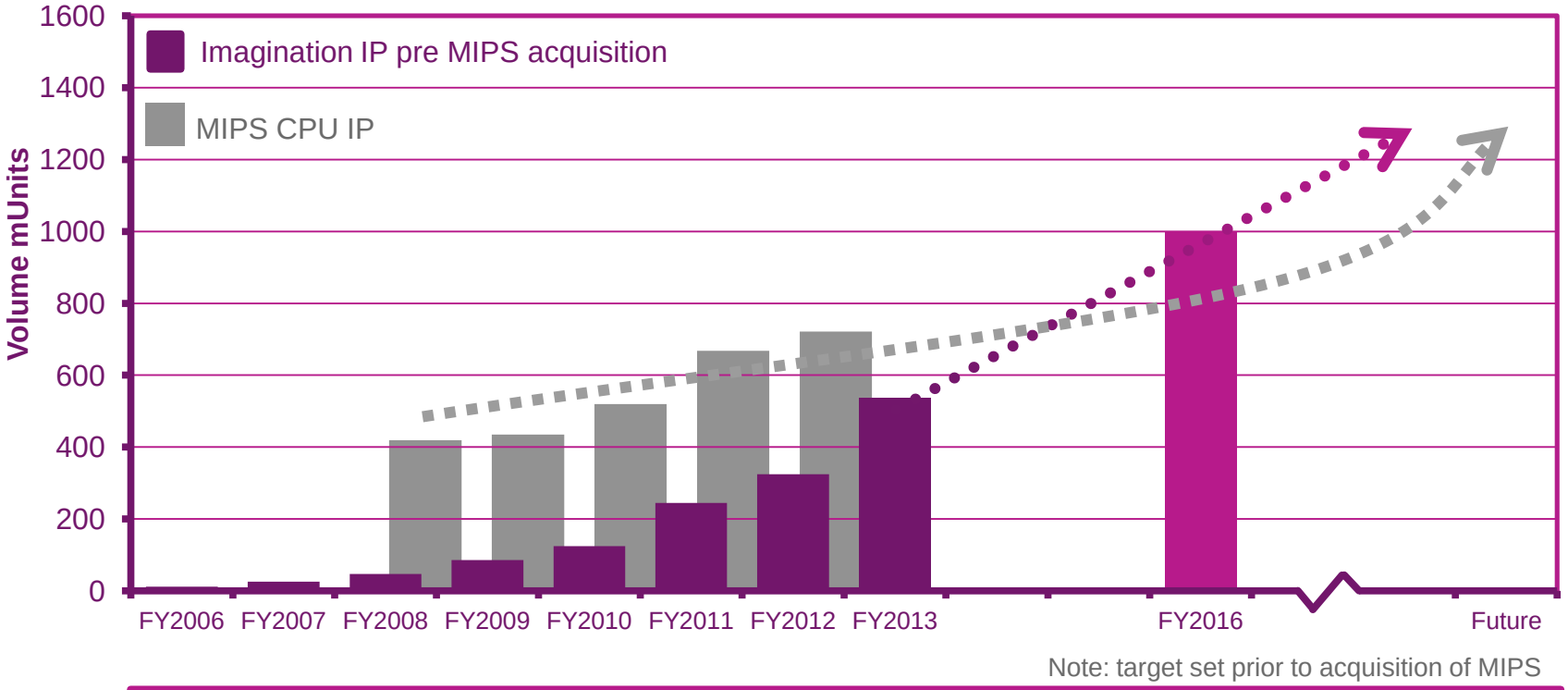
Licensable IP will be announced and available shortly – strong interest already

Business Momentum

Strategic progress

- Strong licensing activity across our portfolio
- Strengthening deployment of PowerVR Series6 GPUs
- Ray tracing technology gaining interest
- New Vision processor opens up new opportunities
- MIPS Series5 P5600 CPU demonstrates performance leadership, full feature set
- Google PNaCl in Chrome OS, ART (beta) in Android 4.4 confirms move to app portability across CPU ISAs
- Ensigma powered devices for both TV and Wi-Fi entering volume production
- FlowCloud technology attracting new partners

Scaling the business to the next level…

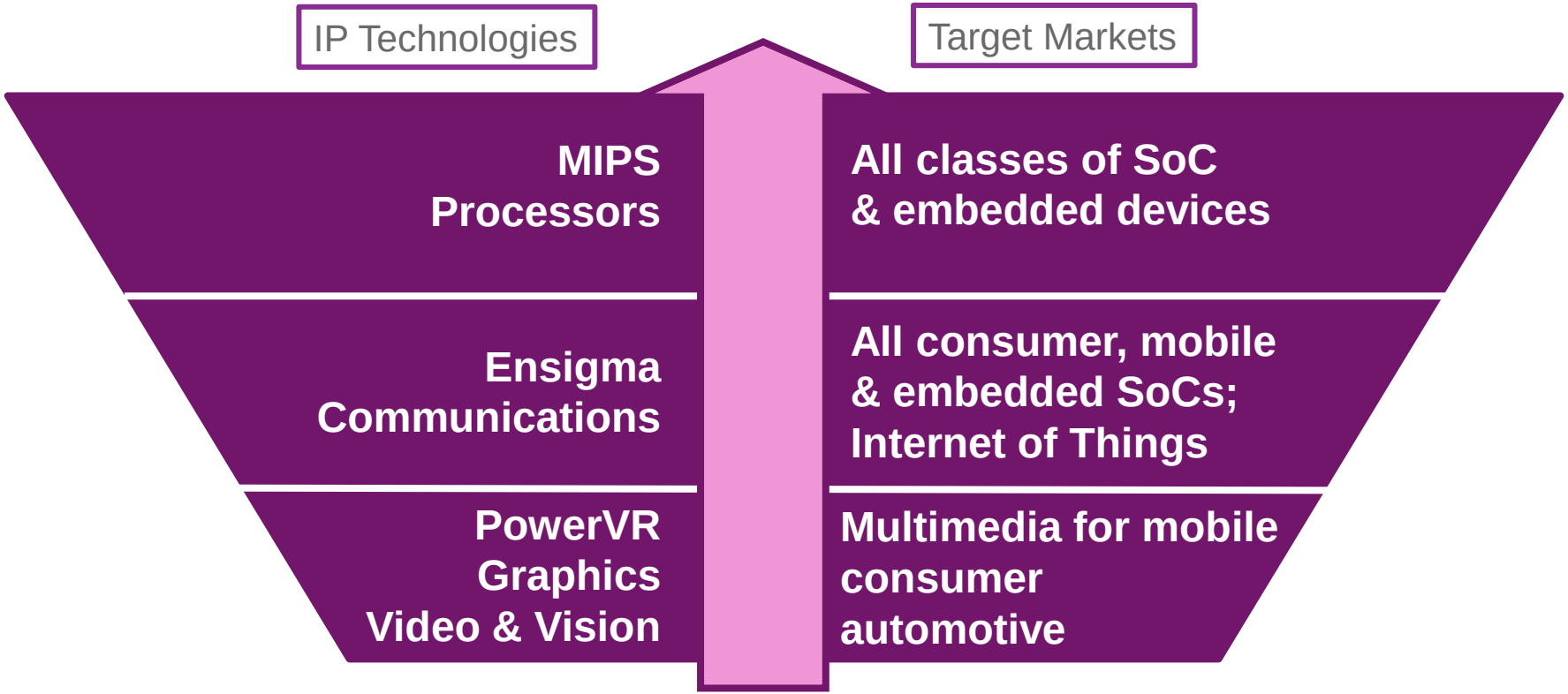


Note: target set prior to acquisition of MIPS

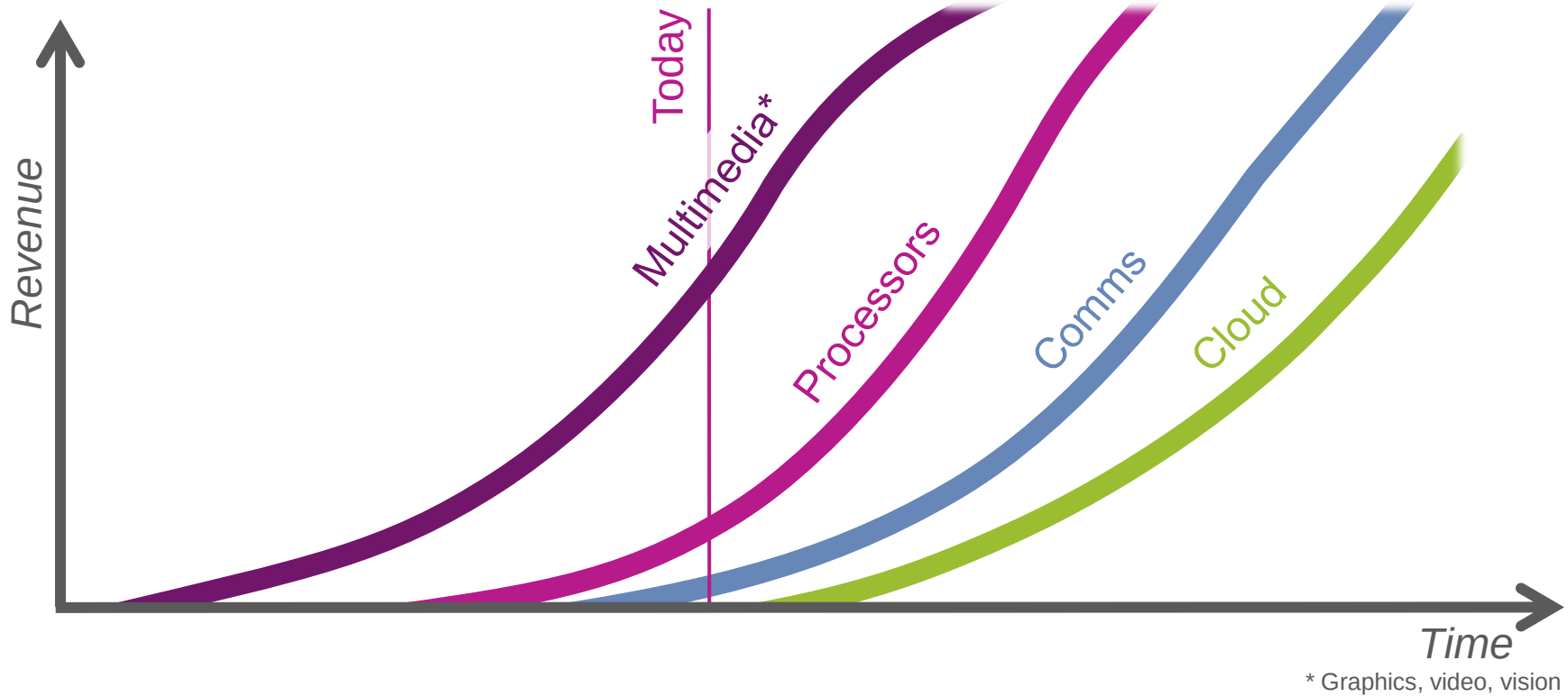
Our goal has been to achieve around 1 billion units/annum shipments…

Broadening our TAM

Each step of our IP technology expansion takes us into new & larger target markets



Driving multiple revenue streams



* Graphics, video, vision

Our markets are growing

IoT in early days – further potential for billions of units

Market Segment	TAM* 2017 M Units	SAM** 2017 M Units	Potential Share of SAM	Categories
Mobile Phone	1,570	1,400	35%-60%	*Smartphones*
Home Consumer***	895	703	20%-50%	*All TV, radio, connected audio; media players, cameras, games consoles*
Mobile Computing	912	724	30%-50%	*Tablets, ultra mobile PCs, laptop PCs*
In-car Electronics	210	176	15%-30%	*Navigation, PND, dashboards, head-units*
Networking	1,982	903	30%-50%	*Access points & CPE, enterprise, servers*
Wearables	139	120	30%-50%	*Watches, fitness, home monitoring, eHealth*
Total	5,708	4,026		

** TAM = Total Available Market in the segment (e.g. total number of handsets per year)*

*** SAM = Serviceable (by Imagination) Available Market in the segment (i.e. the number of "non-captive" chips that could use Imagination's IP)*

**** now includes Handheld Multimedia*

Imagination – at the heart of the future

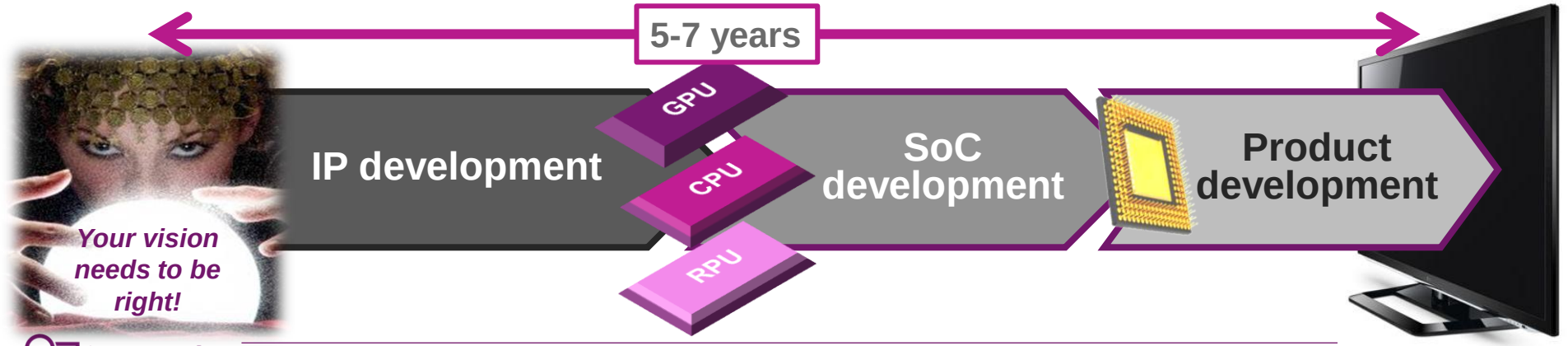
- **Imagination's technologies are integrated into many leading reference platforms in every major market segment**
- **Our ecosystems are large and growing**
  - developers focus on Imagination-based platforms first for the most innovative content
- **We have the best technology – performance per mm2 and per mW**
    - Driven by innovation and real uniqueness
- **We are partner-focused**
  - deep and long term relationships

Technology Trends

From IP cores to SoCs to end products

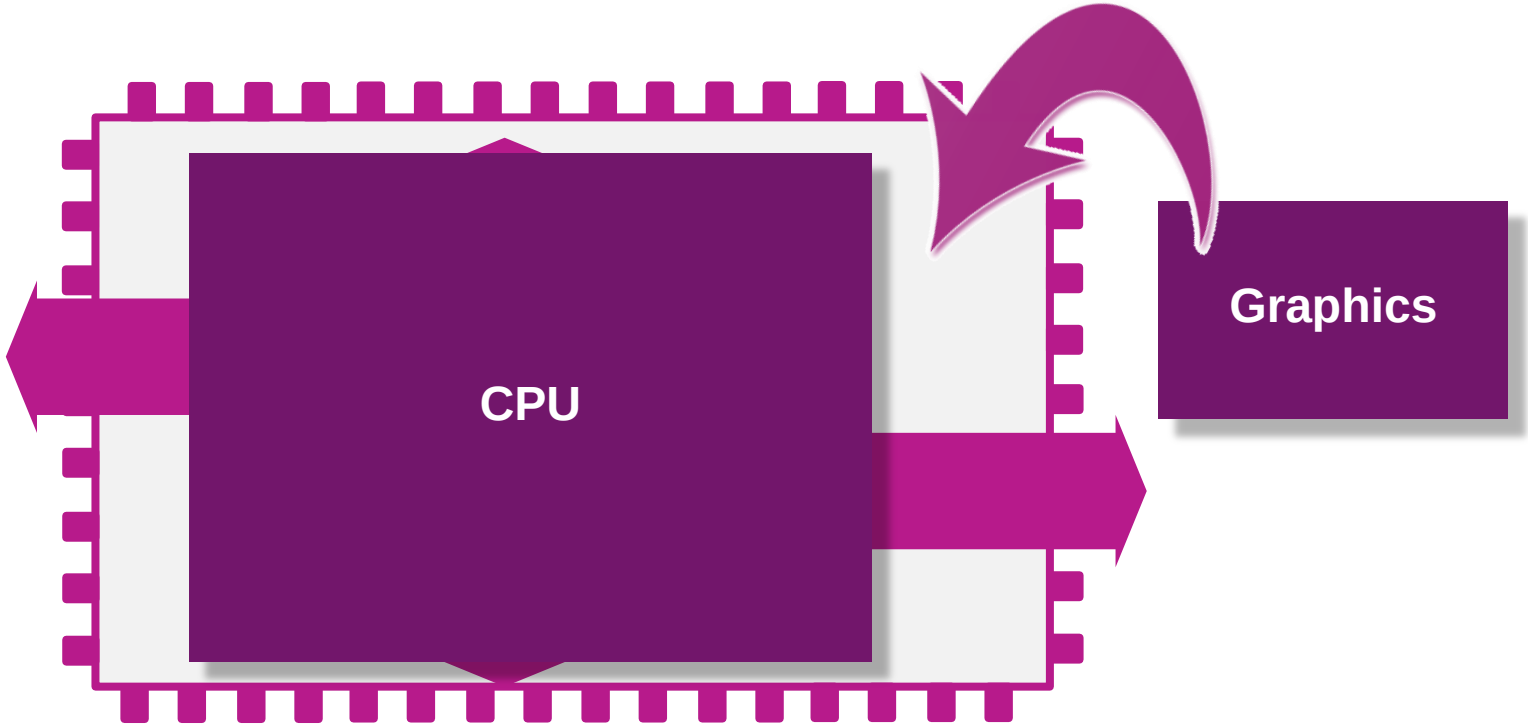
A long innovation path

- **End product features massively influenced by SoC capabilities**
  - SoCs define what an end product can or cannot do
  - End products have around 1+ year concept to launch cycle times
- **SoCs enabled by IP cores**
  - New SoCs have 2+ year design start to production cycle times
- **Complex IP cores take at least 2-3 years to develop**



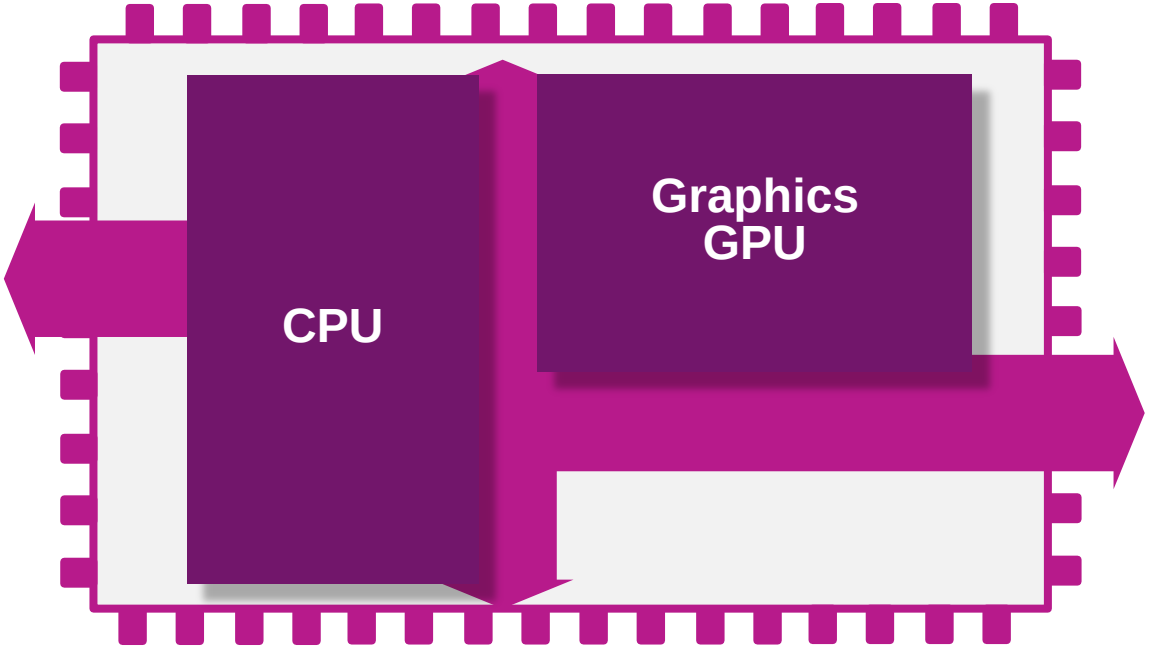
The evolution of SoCs

We said that GPUs would go on chip: “teeth will be provided”



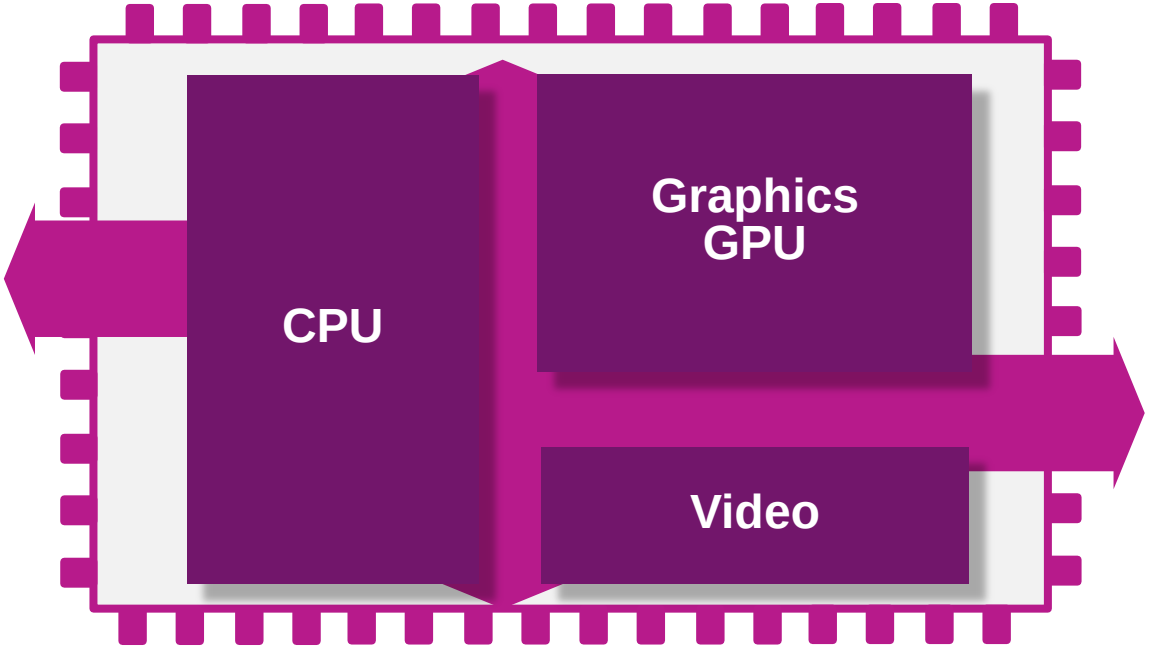
The evolution of SoCs

We were right about that for mobile – and elsewhere



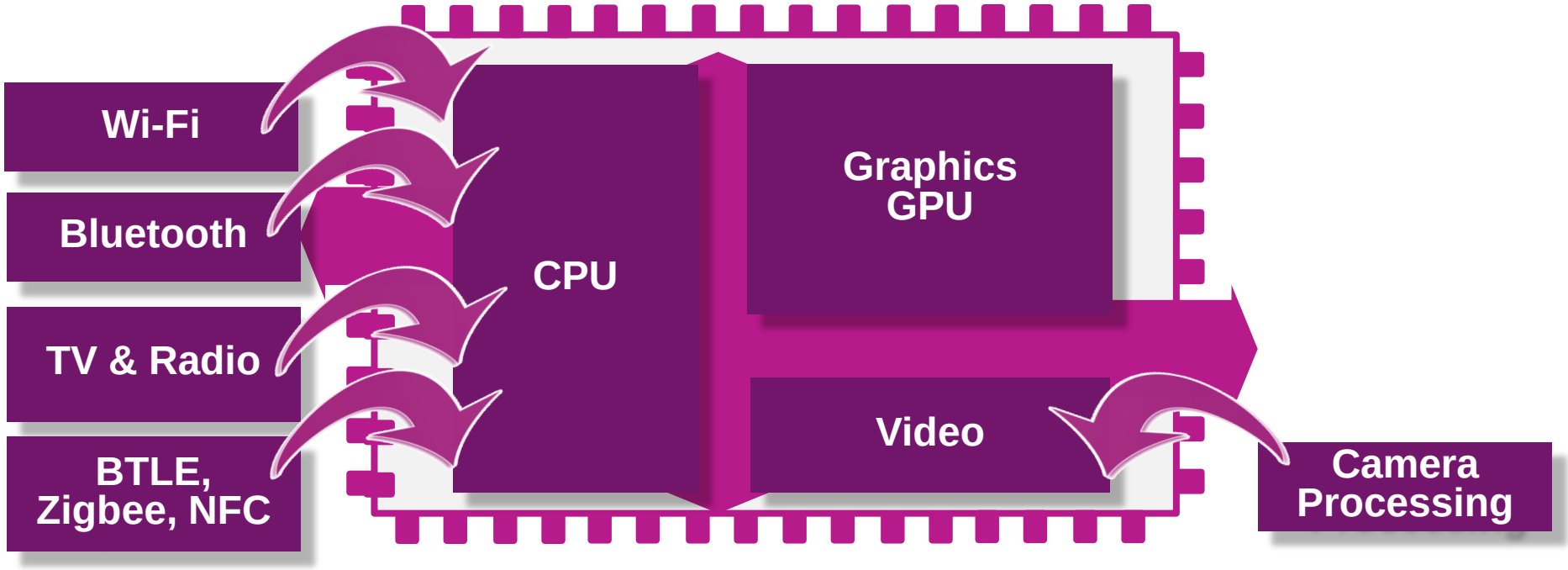
The evolution of SoCs

Video goes hand-in-hand with graphics



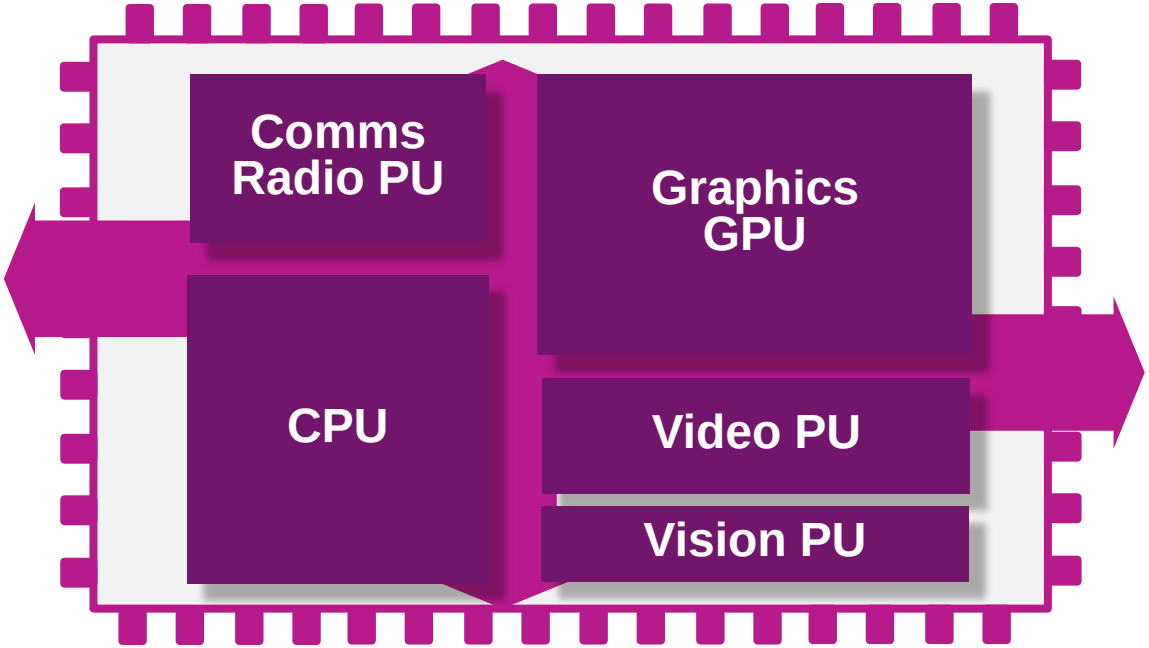
The evolution of SoCs

The next trend: all comms and multi-sensor vision will go on-chip too



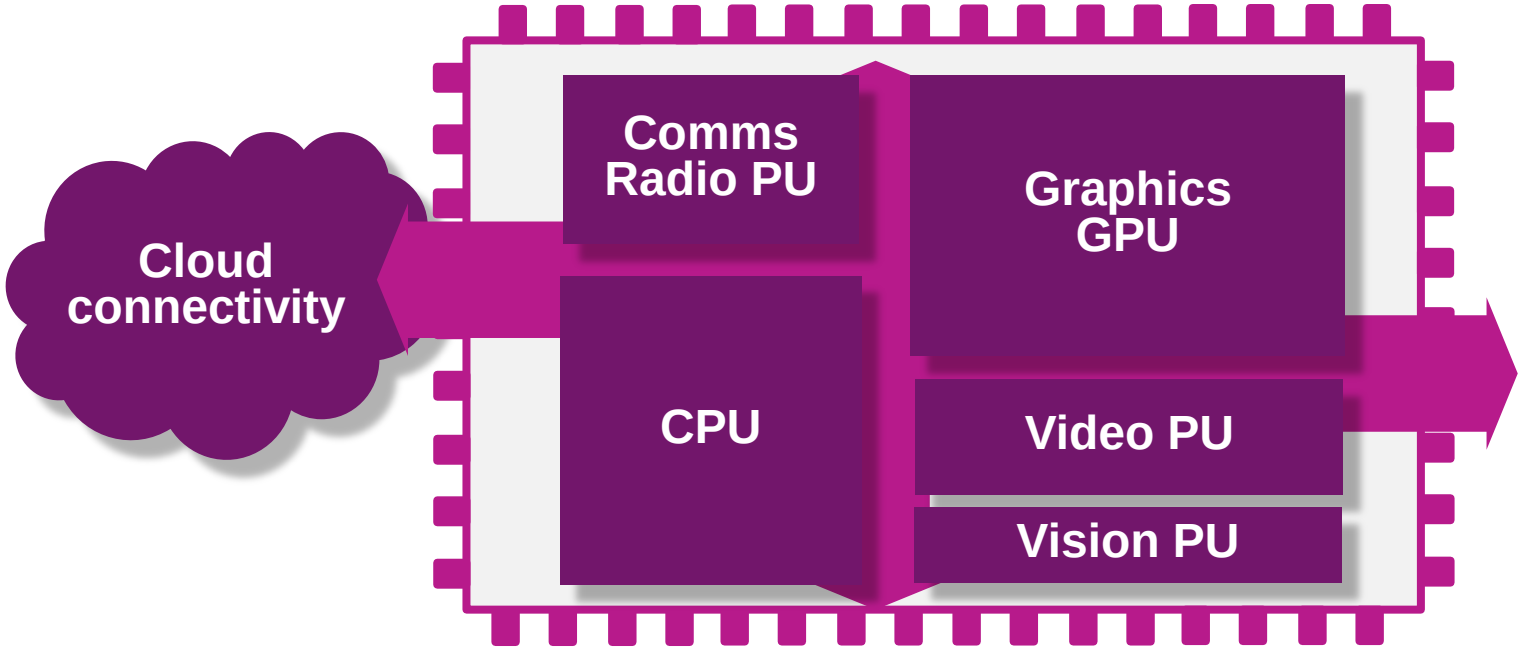
The evolution of SoCs

Additional programmable processor units (PUs) are essential



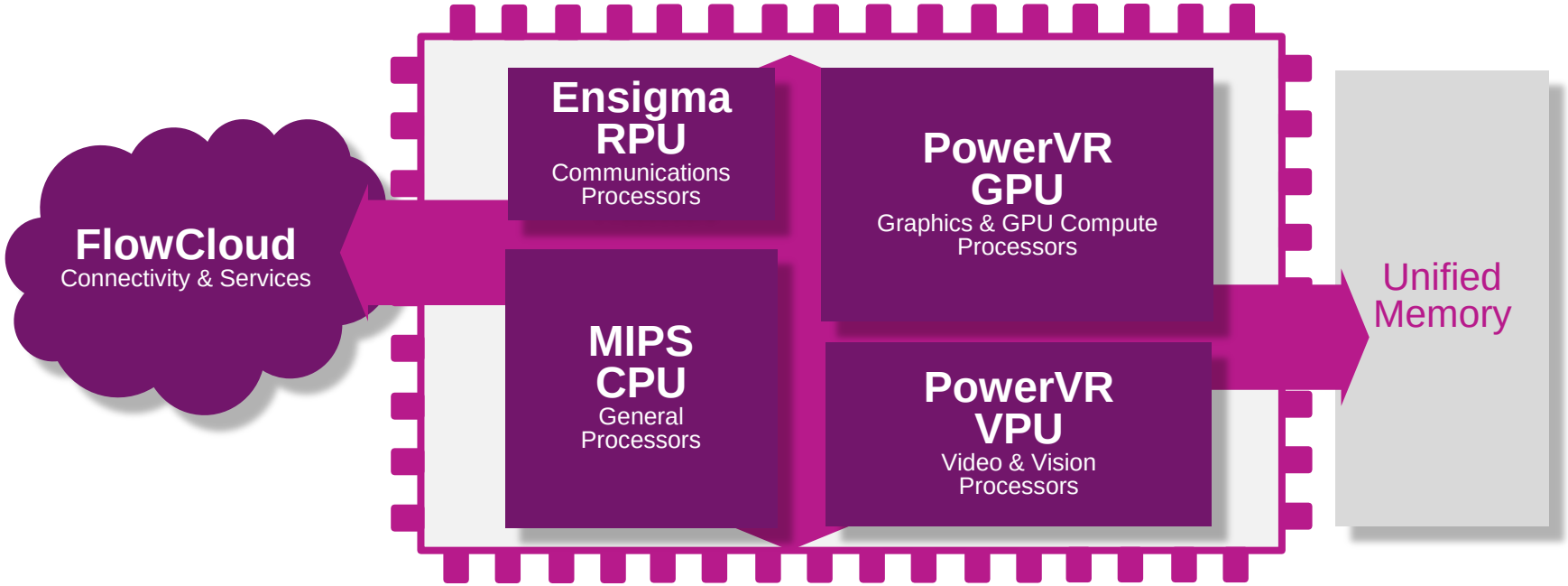
The evolution of SoCs

Connecting devices to the cloud and to each other is also essential



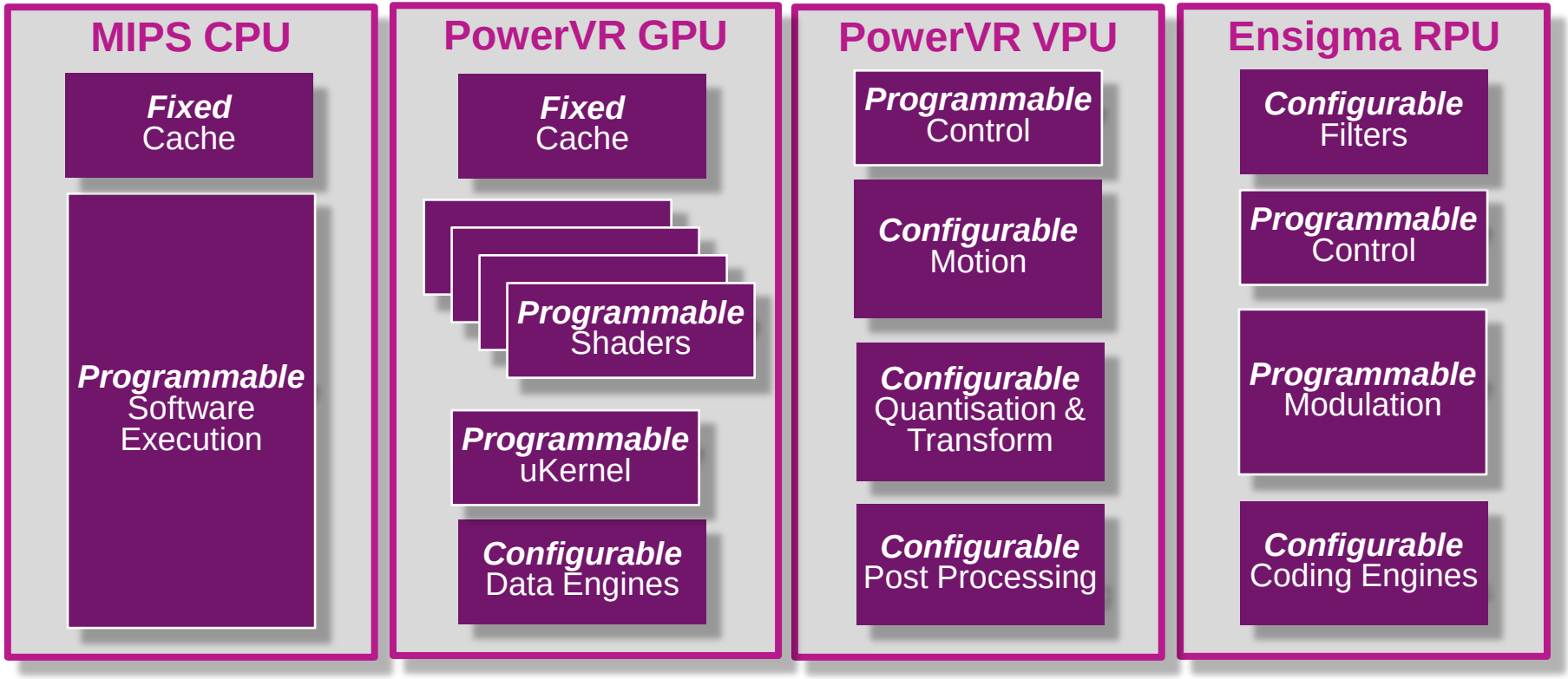
The result: Imagination's IP portfolio

Everything needed to create connected SoC solutions



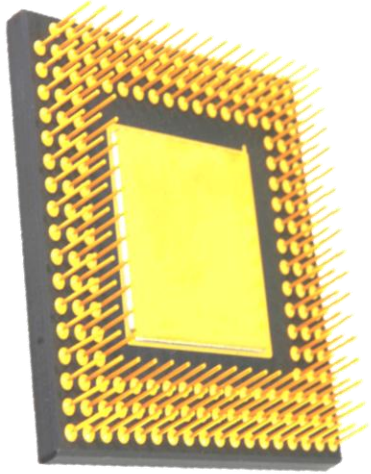
Each processor's architecture highly tuned

Optimised blend of programmable, configurable and fixed function hardware



Each processor designed to be the best

Class-leading functions that join together to create optimal system solutions



CPU: control

- Serial compute for complex sequential heuristics
- System level management and control
- Supports multiple operating systems

GPU: graphics

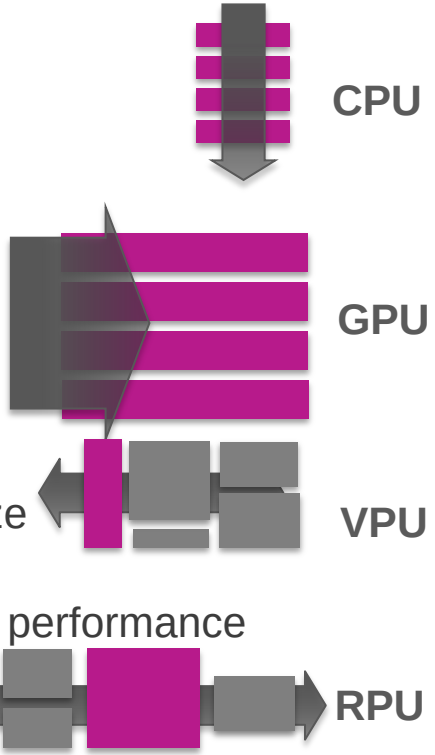
- Both graphics & parallel compute
- Maximum processing on-chip
- High memory latency tolerance

VPU: video

- Multi-standard video decode and encode
- Configurable hardware for ultra-low power and size

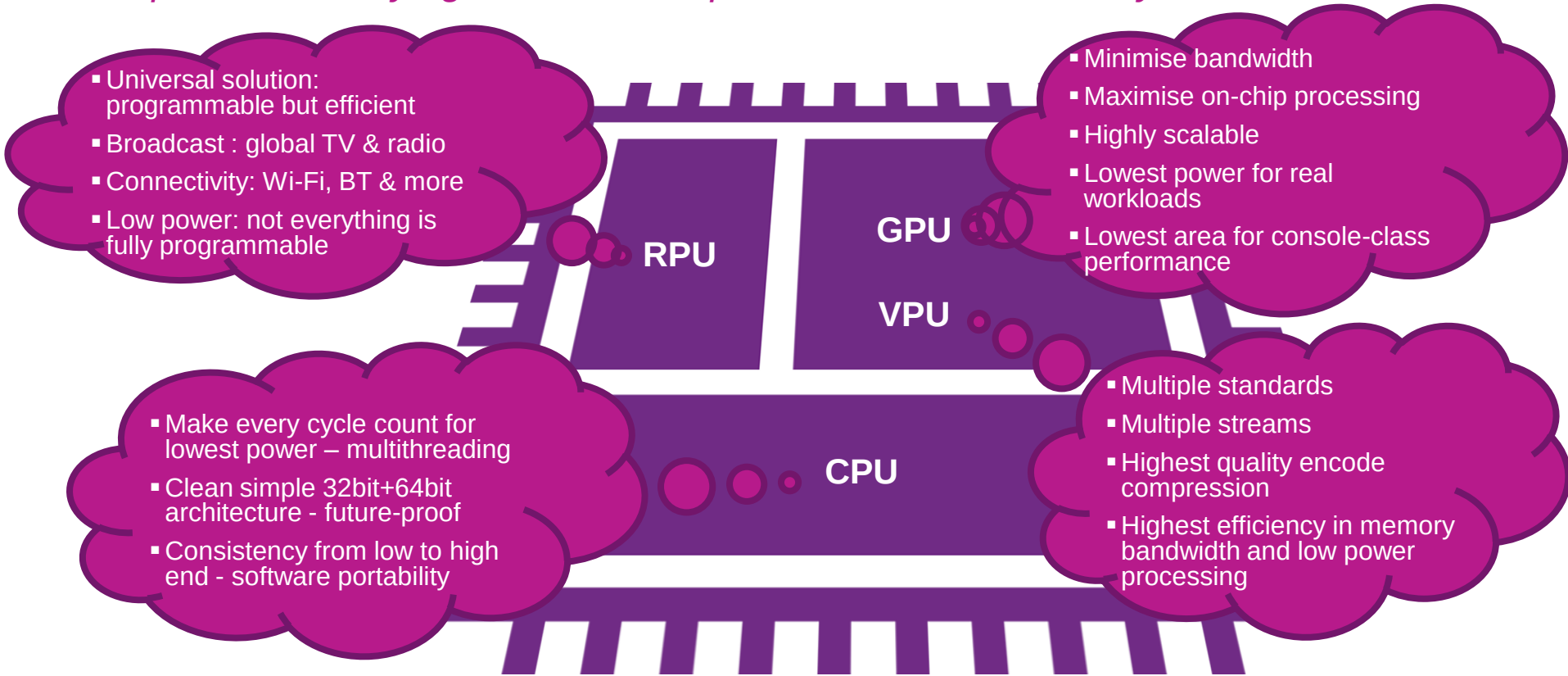
RPU: radio

- Programmable + configurable engines for highest performance
- Complex dataflow at high data rates
- Multi-standard: Wi-Fi; TV/radio; M2M sensors



We have a strong track record

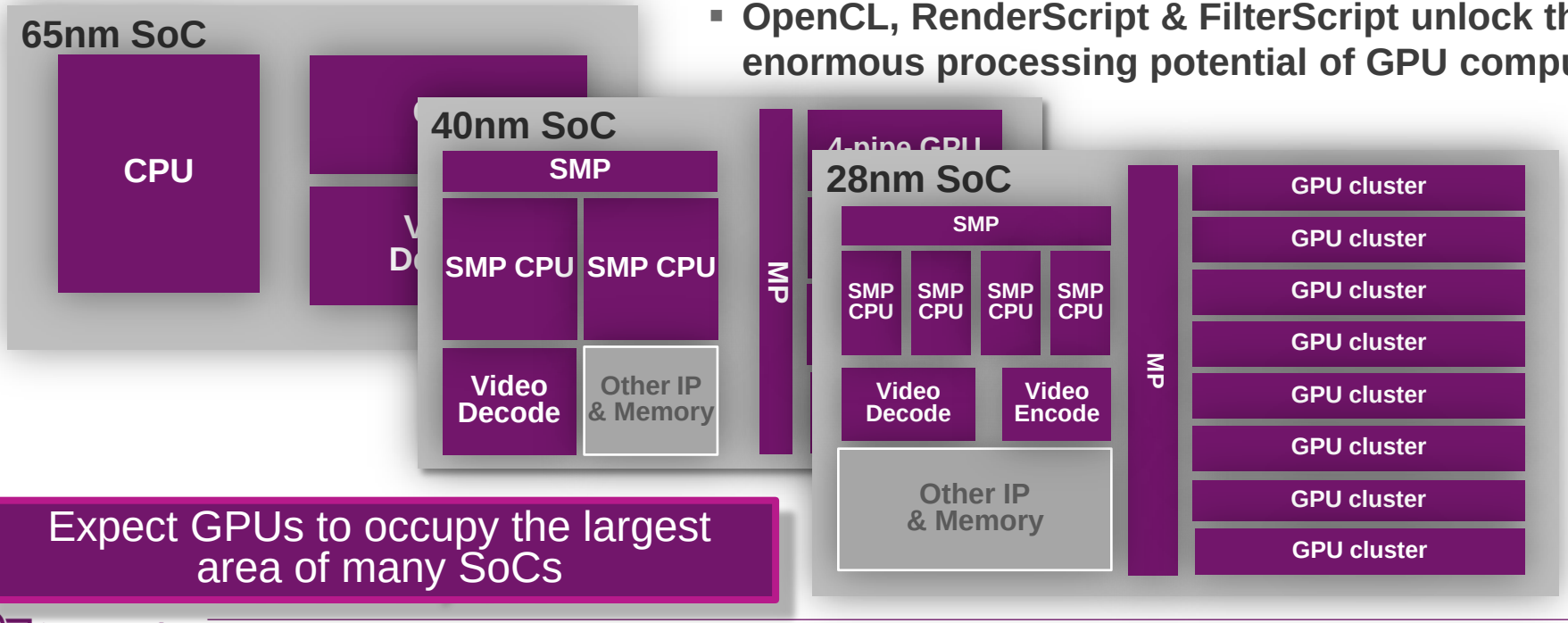
SoC specs & underlying IP must anticipate end user trends 5+ years ahead!



GPUs: increasingly dominating SoC processing

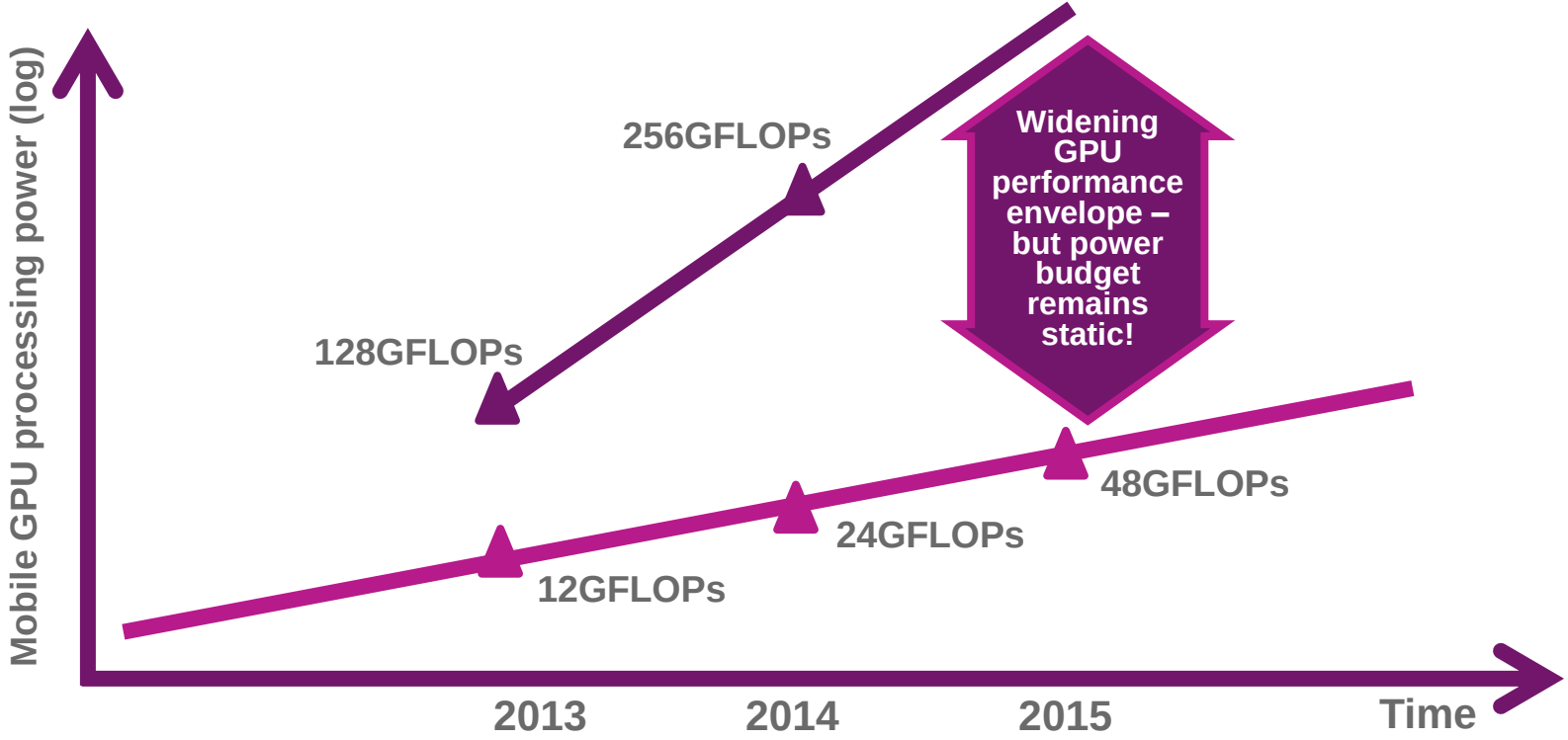
GPUs: data parallel architectures

- Touchscreen displays and graphics powering latest user interfaces and applications
- GPUs are inherently more scalable than CPUs
- OpenCL, RenderScript & FilterScript unlock the enormous processing potential of GPU compute



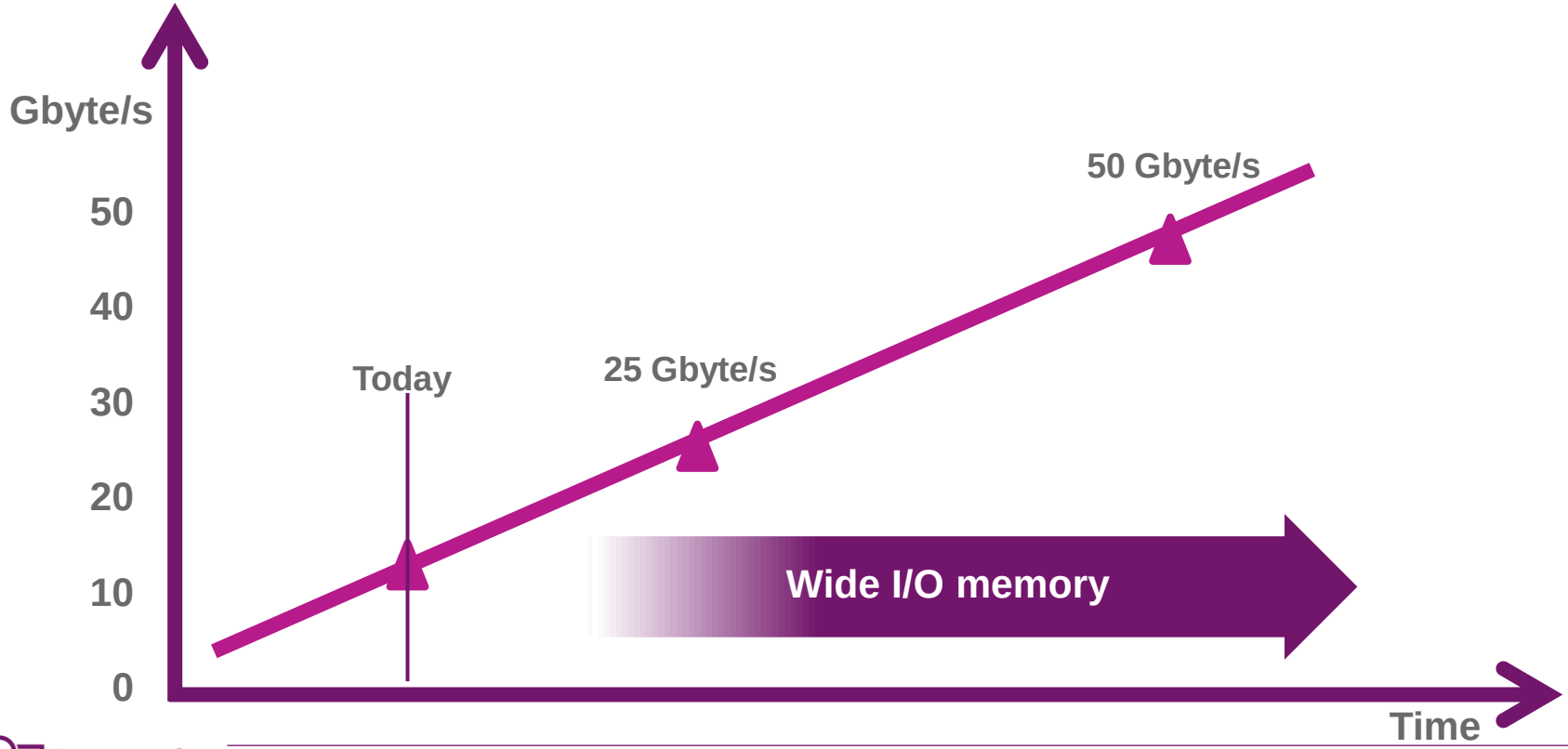
Expect GPUs to occupy the largest area of many SoCs

GPU performance: faster yet lowest power



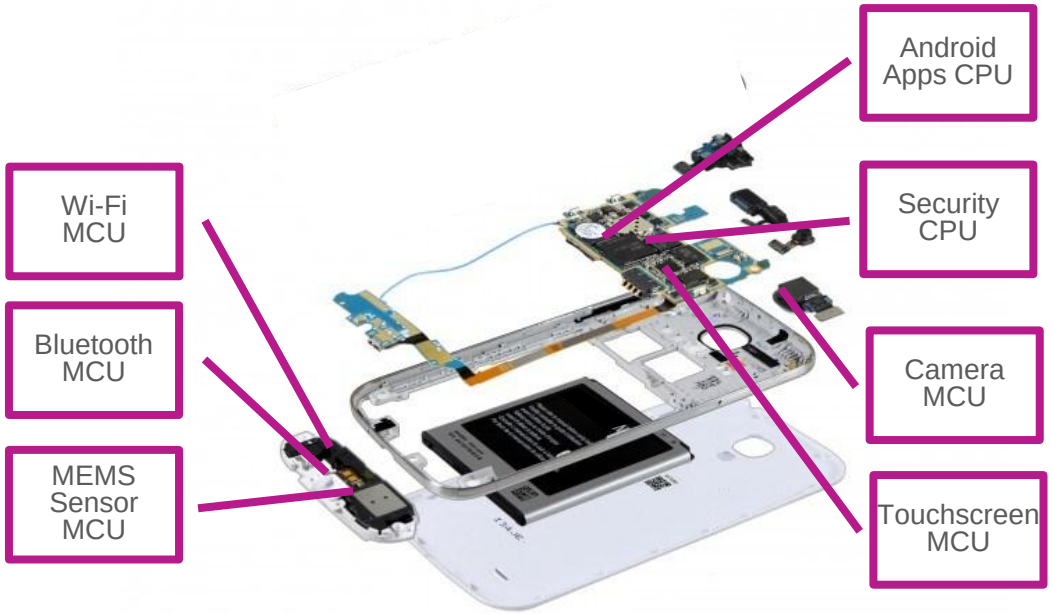
GPU processing increasing >2x per year – for both low and high-end
Envelope of GPU performance widening ~2x per year between low and high-end

SoC memory bandwidth: another enabler



CPU IP is an broad & diverse market

Every product has many types of CPUs and MCUs



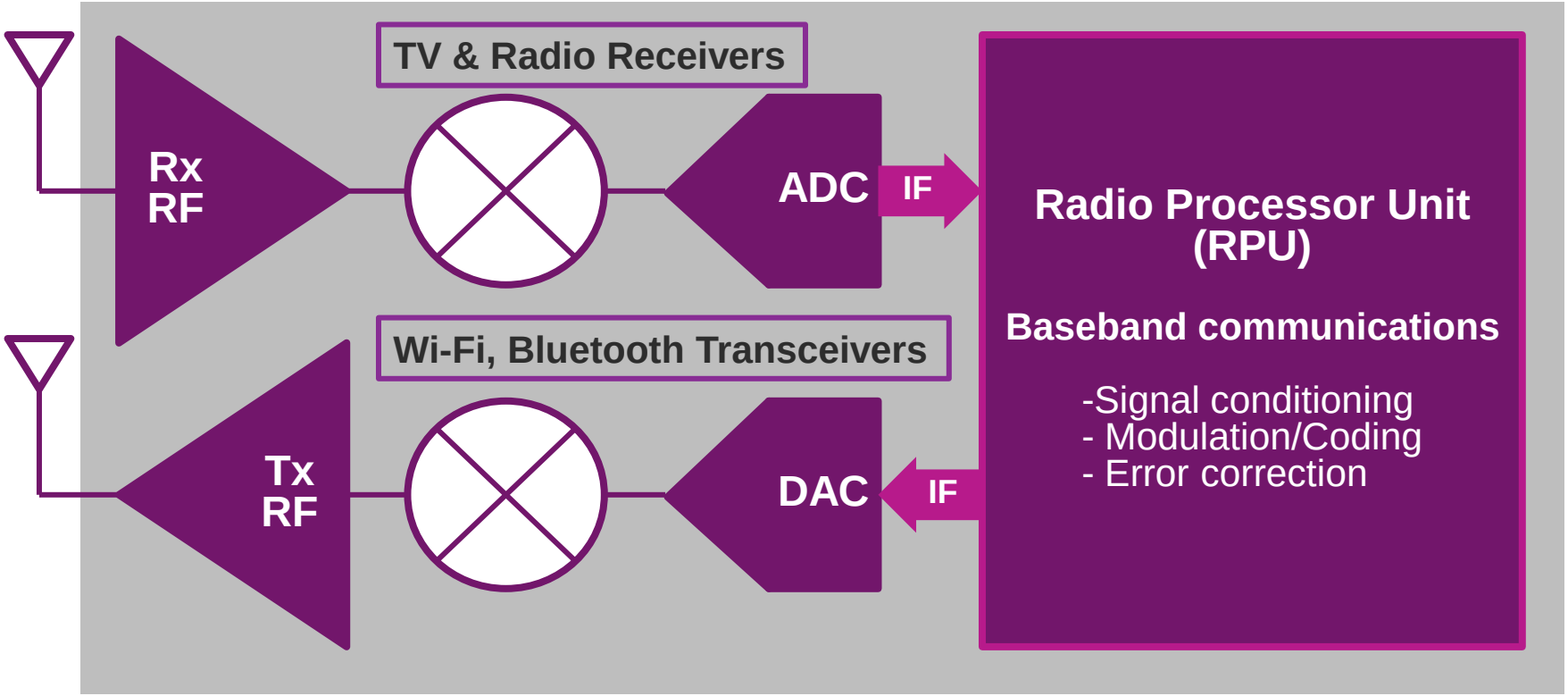
Note: Example CPUs and MCUs are for illustrative purposes only; they do not necessarily reflect actual positions or functions in actual device shown

- **64-bit becoming the new standard for high end processors**
- **Binary compatibility is key for 32 to 64 bit evolution**
- **32-bit becoming increasingly popular even in low end microcontrollers (MCUs) as everything needs connectivity**
- **Multi-core, multi-threaded, virtualization, security, FPU, DSP/SIMD all becoming expected features in high end CPUs**

CPUs are everywhere – it's an enormous and growing IP market
As everything gets smarter, even the smallest CPUs are moving to 32-bit

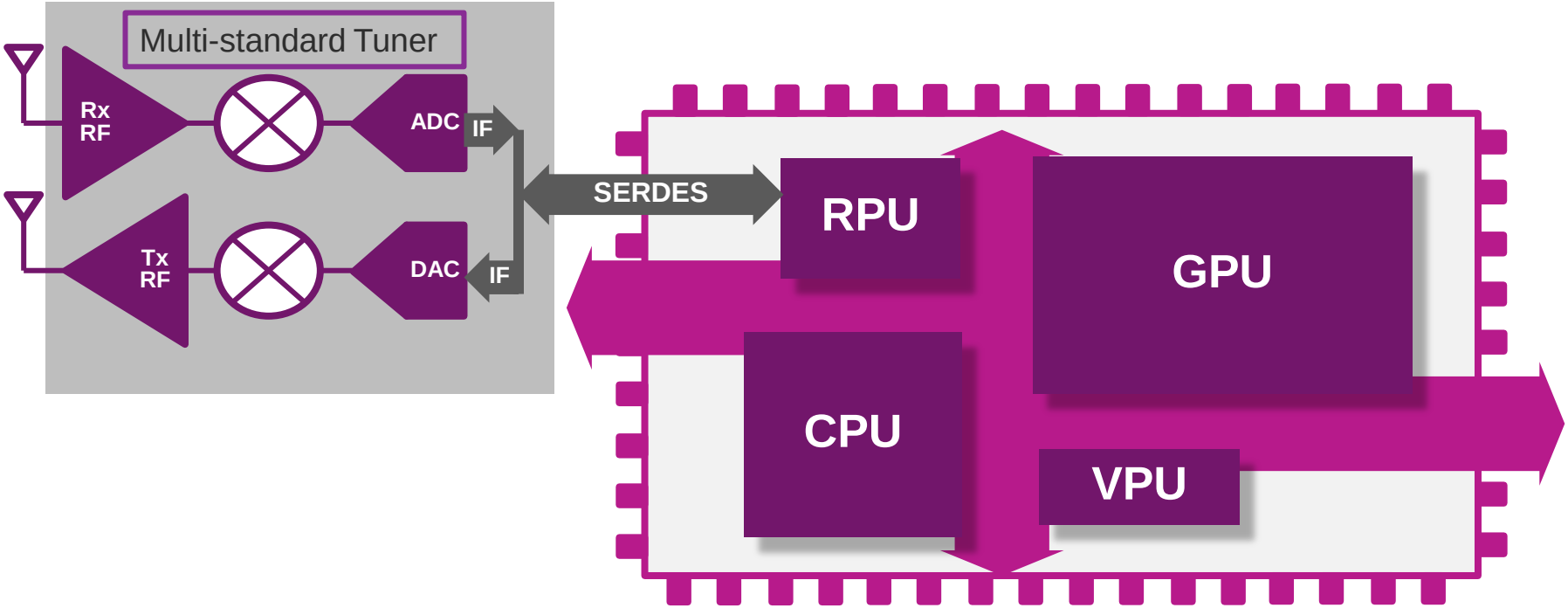
Connectivity integration for cost-sensitive SoCs

RF to baseband on-chip for highly cost-optimized embedded applications



Connectivity integration for flexibility & upgrades

Using SERDES to digital tuners, OEMs can qualify RF for multiple SoCs



The “Internet of Things” will reach everywhere

Everything is getting “smart”

Computer

Phone

TV/Radio

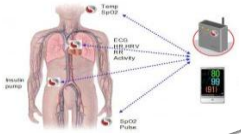
Car

We need connected solutions for everything!

Ensigma MIPS PowerVR Flow HelloSoft

…and more to come…

Healthcare



Security

Home Automation

Toys

Industrial

Everything!

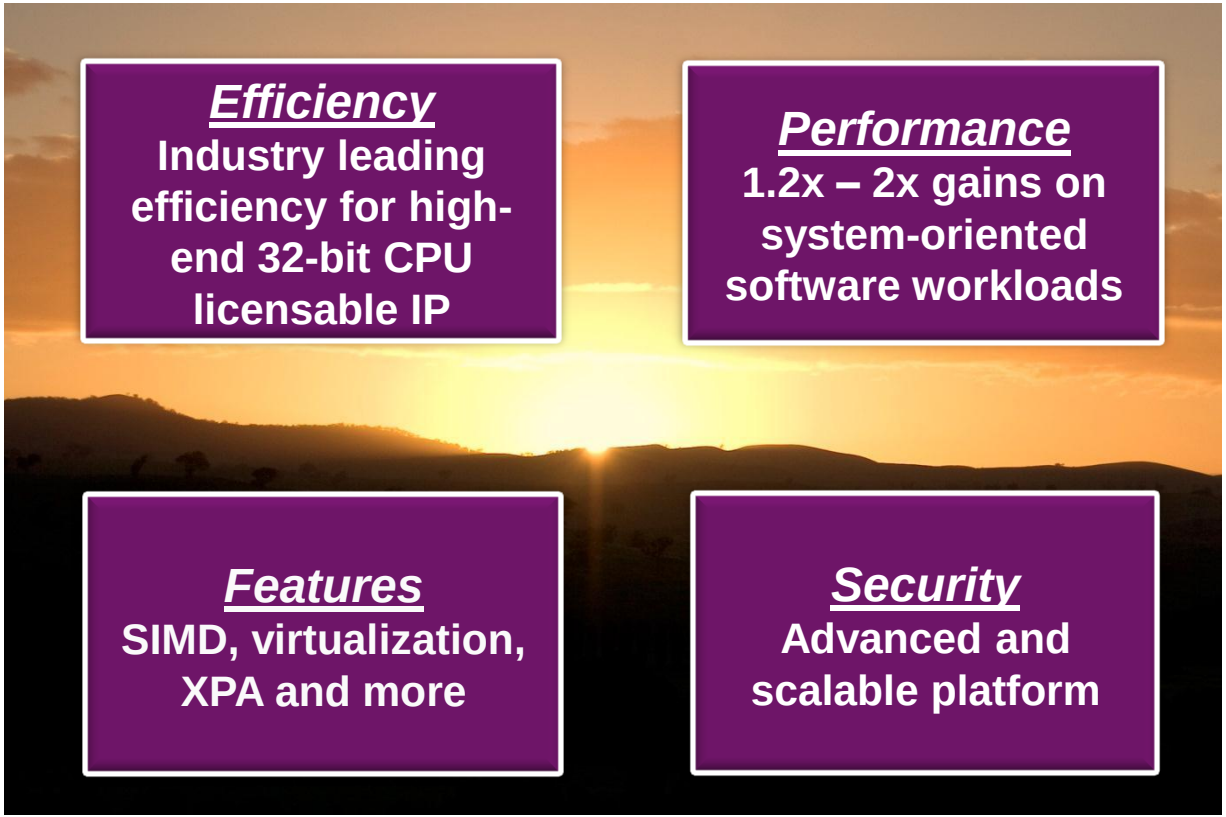
MIPS CPU Processor Solutions: Enter the Warrior

Mark Throndson
Director of Processor Technology Marketing
Mark.Throndson@imgtec.com

www.imgtec.com

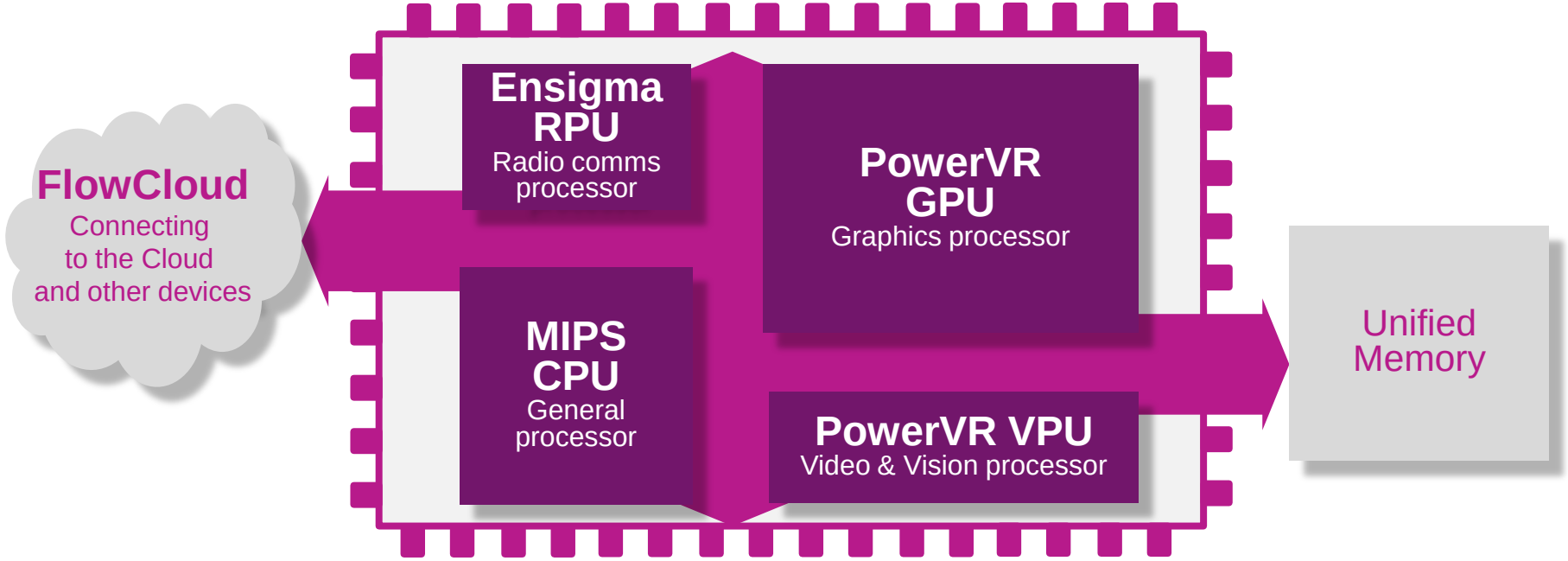
Enter the ‘Warrior’

Unleashing the first MIPS Series5 CPU IP core: P5600 for leading 32-bit performance



SoC IP for every market

Imagination has the industry's most comprehensive IP portfolio



All of Imagination's IP stand as class leaders in their field, and also work together to create unrivalled solutions for our increasingly connected, media-rich world

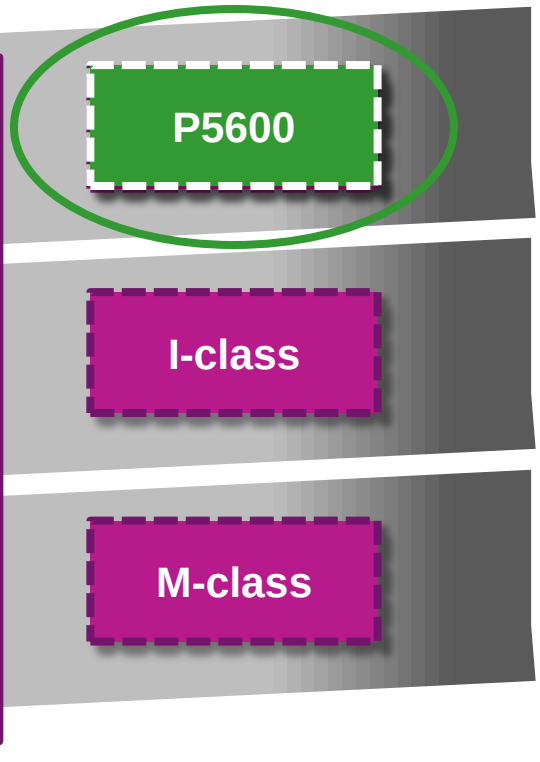
MIPS CPU roadmap

Compatibility and efficiency

Classic

Aptiv

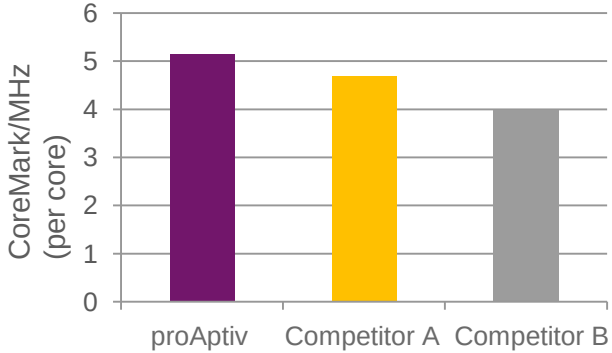
- Proven MIPS architecture used for 30 years
- Full binary compatibility: low end 32-bit to high end 64-bit
- Hardware virtualization
- Architectural support for hardware multi-threading
- Extensive multi-core capabilities
- Advanced SIMD
- Superior security
- Consistent common tool chain
- Extensive 32-bit and 64-bit ecosystems



Leading high-end 32-bit compute efficiency

High end 32-bit designed for future mid-range products

- **Leading performance for licensable IP**

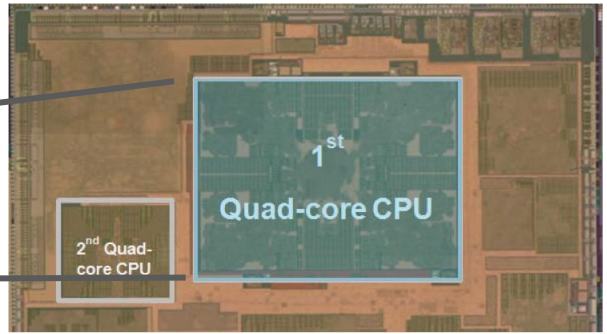


Built with GNU gcc head of tree (4.9) using a gcc plug-in.

- **Efficiently Implemented**

P5600 Quad Core w/2MB L2$

~ 60% core size*
~ 70% cluster size*



Samsung 5410 Exynos 5 Octa

Partial Die photo from Samsung ISSCC 2013 Presentation. Cortex A15 cluster highlighted

* Targets based on preliminary implementation details in TSMC 28HPM – subject to change based on final RTL

MIPS P5600 – leaps in performance efficiency

- vs. proAptiv at same frequency and silicon process*
  - 1.2x-2x faster on system benchmarks
    - SPEC, LinPack, MultiBench, Javascript, Browsers …
  - 2x-3x higher data movement
  - Similar power envelope

- 1 GHz -> 2+ GHz implementation range in TSMC 28HPM

* Performance metrics based on preliminary implementation details – subject to change based on final RTL

MIPS P5600 market segments – mobile and others

Full featured for broad market applicability

Mobile

- Mainstream smartphone & tablet apps processor

Home Entertainment

- Mainstream DTV/STB/BD processor

Networking

- Res. Gateway
- 802.11ac
- CPE Modems
- Network Appliances

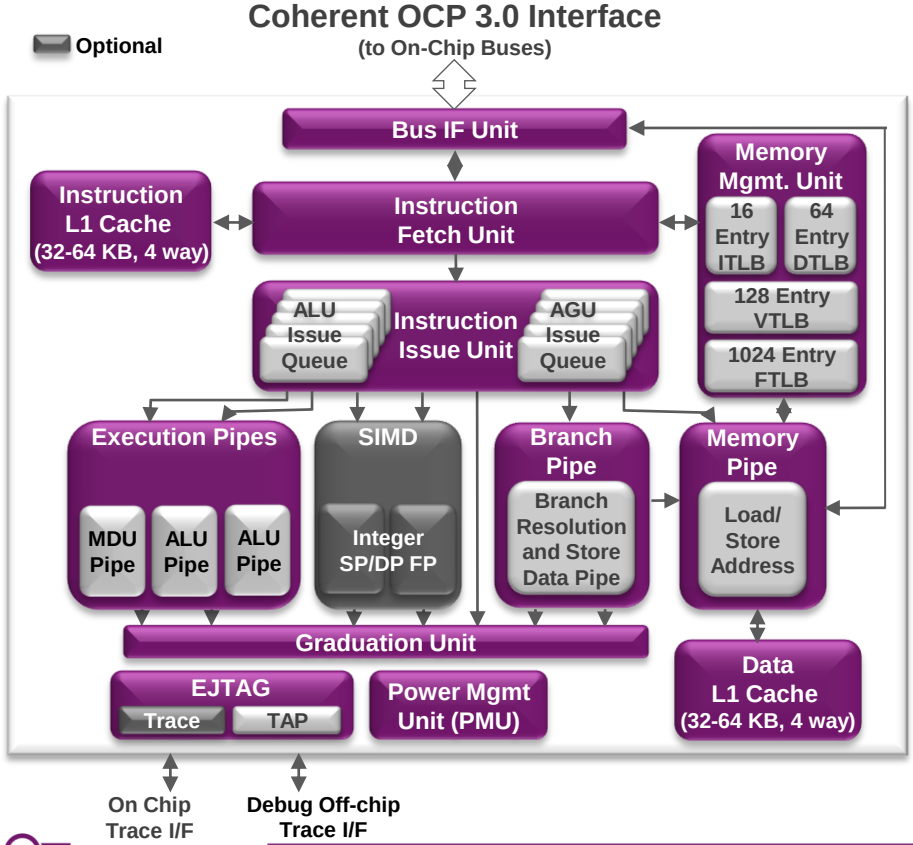
P5600 – designed for modern application software

Large, highly complex, OS and virtual machine workloads

- MIPS ISA – purer RISC ideal for dynamic compilation
- Best in class branch prediction
- TLB resources – > 1000 entries to minimize large code page refills
- Enhanced Virtual Address(EVA) + 40b Extended Physical Address (XPA)
- Coherent multi-core configurations up to 6 cores
- Hardware Virtualization and SIMD


MIPS P5600 base core microarchitecture

Optimized for peak single thread performance

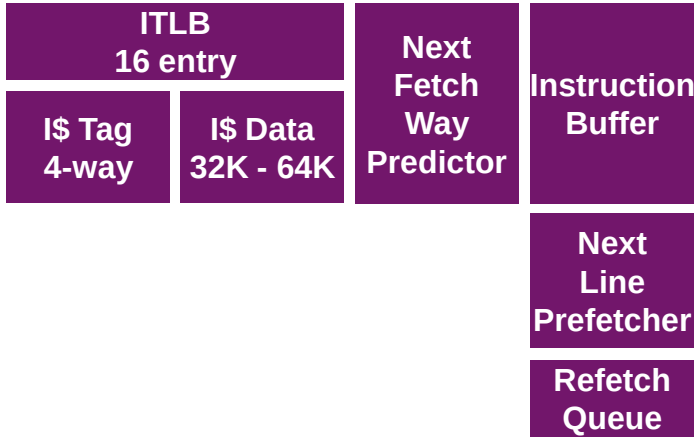


- **SuperScalar (SS) Multi-issue Out-of-Order (OoO) design**
- **16-stage pipeline -> high frequency**
- **Peak instructions through pipeline:**
  - 4x fetch, 3x bonded dispatch
  - 4x integer + 2x SIMD issue
  - Instruction bonding - 6x issue looks like 8x
- **128-bit SIMD (Integer, SP/DP Floating Point)**
- **Widened datapaths, lower latencies**

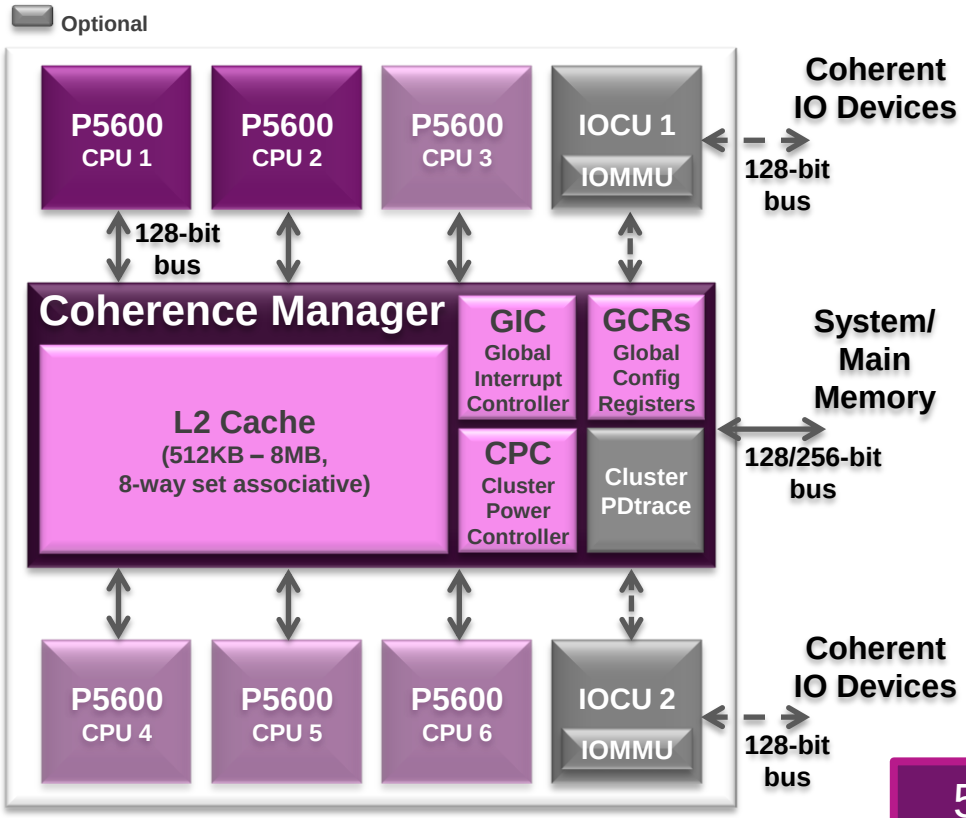
Efficient performance from balanced design

Emphasis on maximum utilization of the pipeline

- **Load/Store instruction bonding – increases memset, bcopy, strcmp, spill-fill, GPU comms**
  - 1 memory pipe looks like 2 - bonds two adjacent 32-bit INT or 64-bit FP accesses per cycle
  - Power + area savings - only 1 DTLB/tag array/single-ported data array, with one access
  - More ILP and MLP – only 1 entry in queues/buffers, only 1 op on L1 miss
- "Right-sized", two simple centralized schedulers
  - Read registers after issue, no reservation stations
- Branch prediction – delivers class leading accuracy
  - BHTs: novel algorithms + sophisticated global history
  - BTBs: multi-level latency/size balance (up to 512 entry x 4-way)
  - JR Cache and RPS: Indirect branch and return predictors



MIPS P5600 coherent multi-core system



- **Enhanced Coherence Manager with L2$**
  - HW pre-fetch, widened busses, reduced latency
  - 128-bit core:CM interfaces; 256-bit CM busses
  - XPA -> 40-bit physical addressing
- **IOCU (1 or 2 blocks) with IOMMU for VZ**
  - Secure I/O processes per virtual domain
- **Global Interrupt Controller with VZ**
  - 256 system interrupts, secure per virtual domain
- **Cluster Power Controller**
  - Clock and Voltage domain/gating per core
- **PDtrace™ – Cluster level prog/data trace**

50K CoreMark, 35K DMIPS @ 1.7 GHz!

MIPS P5600 SIMD highlights

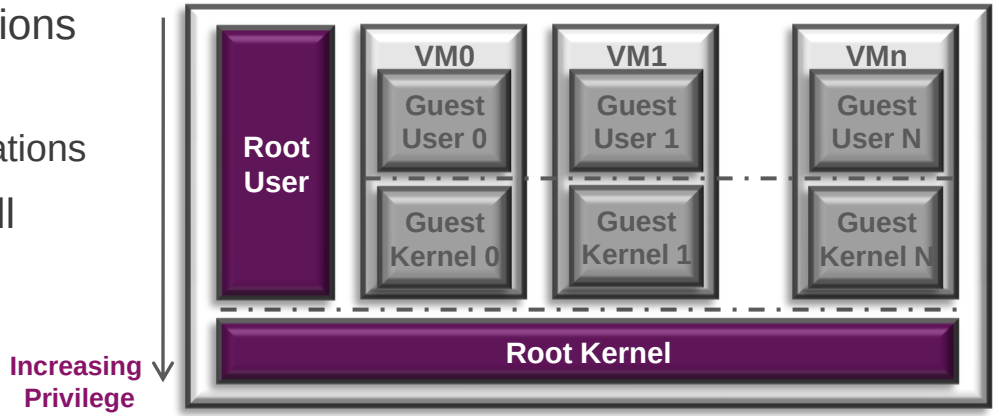
- **For audio, video, 2D/3D graphics, speech, general DSP-oriented workloads**
- **MIPS SIMD - 150+ instructions consisting of:**
  - Integer/fixed point/floating point arithmetic, compare/convert, branch/move
  - Permute and arbitrary shuffle (arrangements) on vectors (1D) and arrays (2D)
- **Designed for high-level language programming – easy to support with C or OpenCL**
- **Designed for Performance – 32 x 128 bit vector registers, 128-bit Loads/Stores**
- **Wide range of native data types (8-/16-/32-bit int/fixed pt, 16-/32-/64-bit floating pt)**
- **IEEE-754 2008 compliant**
- **Uniq** **sing**

RISC Philosophy - Efficient Implementation, Compiler-Friendly

MIPS P5600 hardware virtualization

- **Increasing variety of virtualization use cases**
  - Traditional server, Open OS + closed RTOS, heterogenous -> homogenous solutions
  - A foundation for comprehensive, scalable security solutions in a connected world
    - Mobile, consumer, IoT – enterprise/consumer, secure content and transactions, many content sources

- **Key virtualization capabilities – full virtualization with native Guest OS support**
  - Guest and Root have separate TLB and COP0 context
  - Secure isolation of Guest and Root operations
    - Root TLB qualifies guest address translation
    - Hypervisor oversight of Guest privileged operations
  - Hardware table walk ensures fast TLB refill
  - XPA provisions Guest with large memory
  - SoC virtualization with GIC and IOMMU



MIPS P5600 advanced addressing capabilities

- **Enhanced Virtual Addressing (EVA)**
  - Programmable virtual address space segmentation sizes for kernel/user mapping
  - Provides ability to run Linux/OSs in larger footprints (up to 3GB+) without need for HIGHMEM
- **eXtended Physical Addressing (XPA)**
  - 40-bits provides use of physical memory up to 1 Terabyte
- **Hardware page table walk**
  - Fast HW TLB refill essential for greater mapping requirements of XPA, EVA, and VZ
- **Example use case – multi-OS virtualization for microservers/network appliances**
  - 3GB+ per virtual OS domain drives requirement beyond 32-bit PA to 40-bit PA very quickly

First MIPS ‘Warrior P-class’ CPU core

MIPS P5600 CPU summary

- **Major step forward in feature set for high-performance MIPS CPU IP cores**
- **Leading high-end 32-bit performance efficiency**
- **Driven by needs in mainstream mobile and connected consumer markets, with intriguing features for networking**
- **The first in a wave of Series5 Warrior generation CPUs**
  - Processors from high to low setting new standards for CPU IP
  - More Warriors will enter the battle soon!

Available for licensing and silicon design this quarter

The contents of this presentation are **under embargo until 8am CET on Monday, Feb. 24, 2014 (11pm Pacific on Sunday, Feb. 23)**

MIPS Series 5 Warrior M-Class M51xx Processor Cores

February 24, 2014

www.imgtec.com

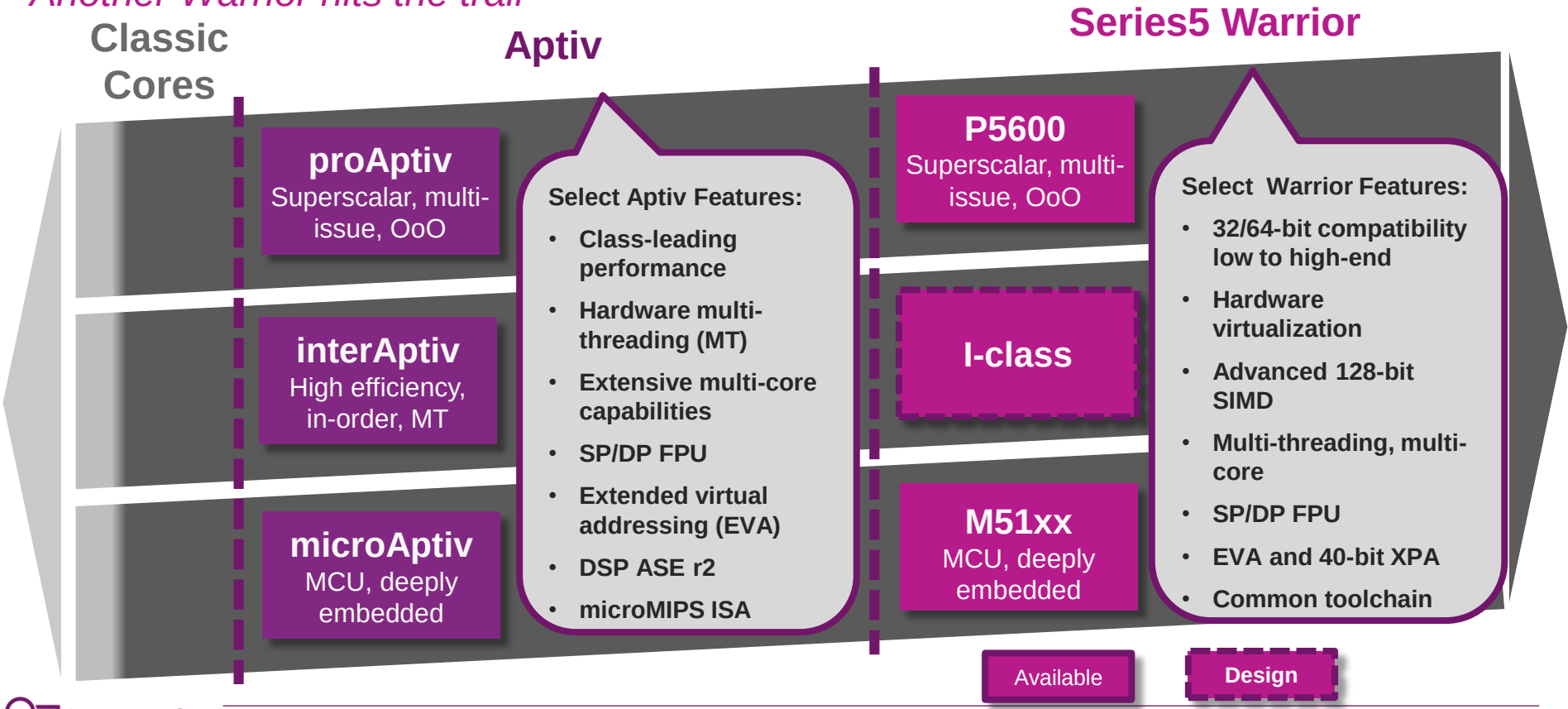
MIPS M51xx: First MCU IP cores with virtualization

Introducing Warrior M-class core family

- **Deliver high performance, security and reliability to entry-level smart embedded applications**
  - Industrial control, IoT, wearables, cloud computing…
- **Optimized MCU and microprocessor versions**
- **Build on popular MIPS microAptiv family**
  - Leading performance and area efficiency
  - Best in class DSP performance
- **Floating Point Unit**
- **Tamper resistance security**
- **Comprehensive development ecosystem**

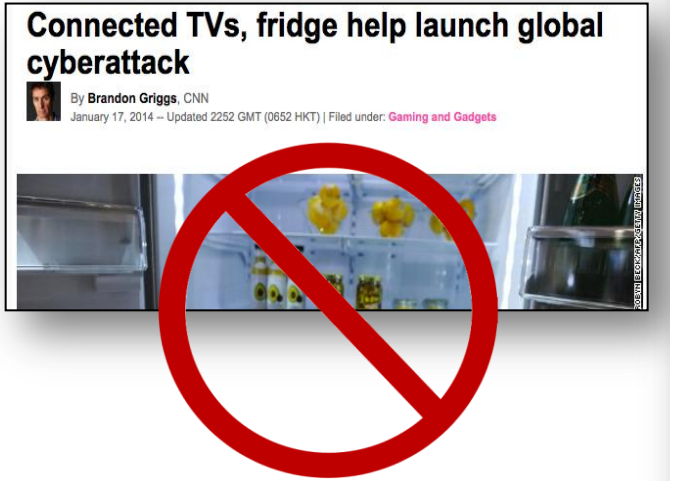
MIPS CPU roadmap

Another Warrior hits the trail



MIPS M51xx: Security in embedded

- Security becoming a ‘must-have’ in embedded systems
- Important in many applications, especially critical for connected products



MIPS M51xx market segments

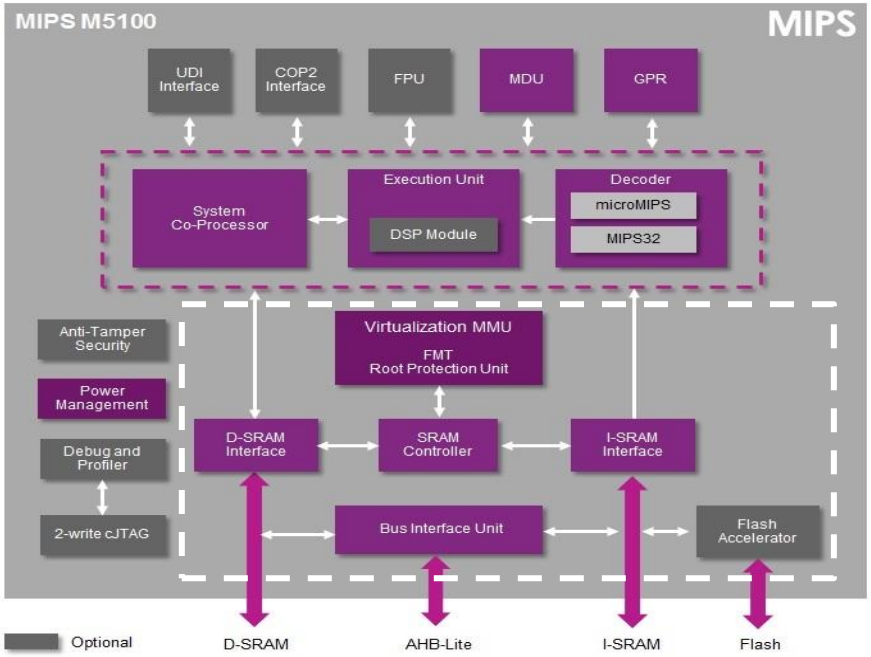
Broad range of digital signal control, secure connectivity and emerging markets

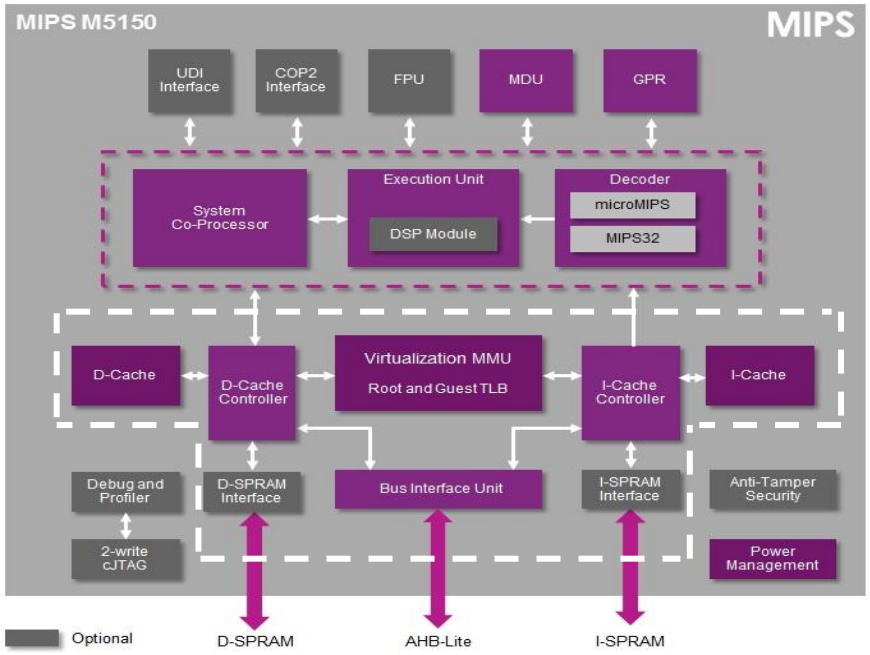
Applications and Use Cases:

- Systems requiring task isolation and secure updates/downloads
- IP protection
- Combine multiple applications on a single, trusted platform
- Safety critical & high reliability systems
- Data collection
- Real-time performance with signal processing acceleration
- I/O controller in a multi-core SoC

MIPS M51xx MCU and MPU versions

Optimized for MCU applications. Performance and area efficient embedded processor





M5100

- **HW virtualization: FMT + Root Protection Unit**
- **I/D SRAM controller**

M5150

- **HW virtualization: Root & Guest TLB**
- **L1 cache controller**

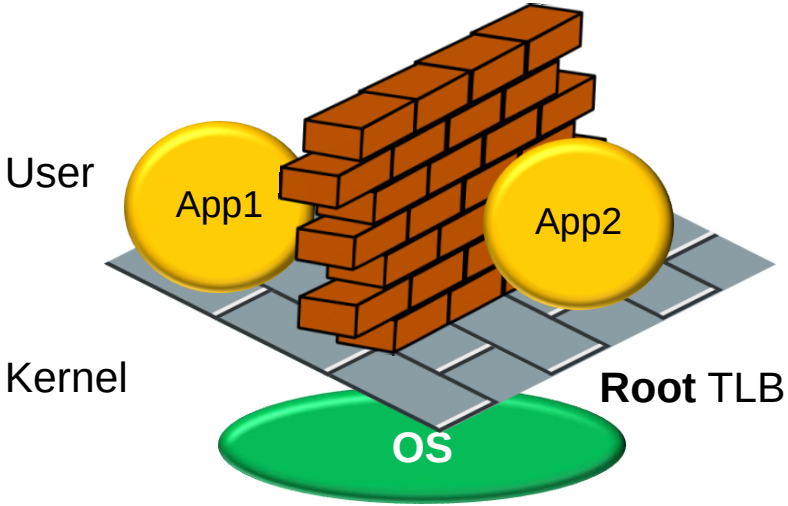
MIPS M51xx common features

Maintaining features from popular microAptiv family CPU cores

- **5-stage pipeline**
  - 3.4 Coremark/MHz, 1.57 DMIPS/MHz. Maximum performance at minimum frequency
- **32 General Purpose Registers**
- **microMIPS ISA**
  - Up to 30% code size reduction
- **DSP & SIMD engine**
  - 150+ instructions, including 70 SIMD and 38 Multiply/MAC instructions
- **Reduced interrupt latency**
  - Delivers real-time advantages
- **Extensive debug and profiling capabilities**
  - Instruction trace, hardware breakpoints, PC sampling, 2-wire cJTAG
- **Power management**

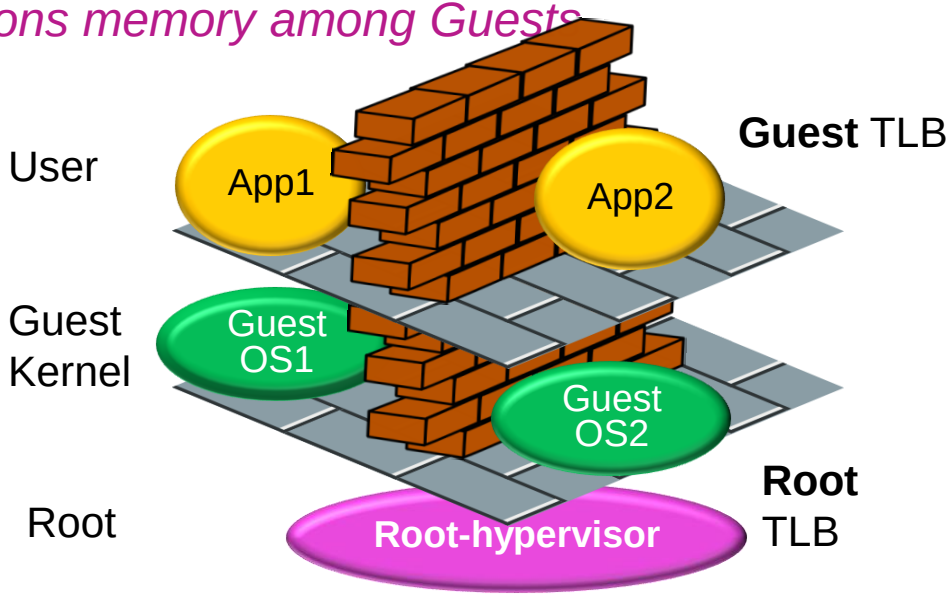
Virtualization in action

Two levels of mapping – securely partitions memory among Guests



Traditional non-Virtualized System

- Single OS with virtual memory
- User App1 & User App 2 protected



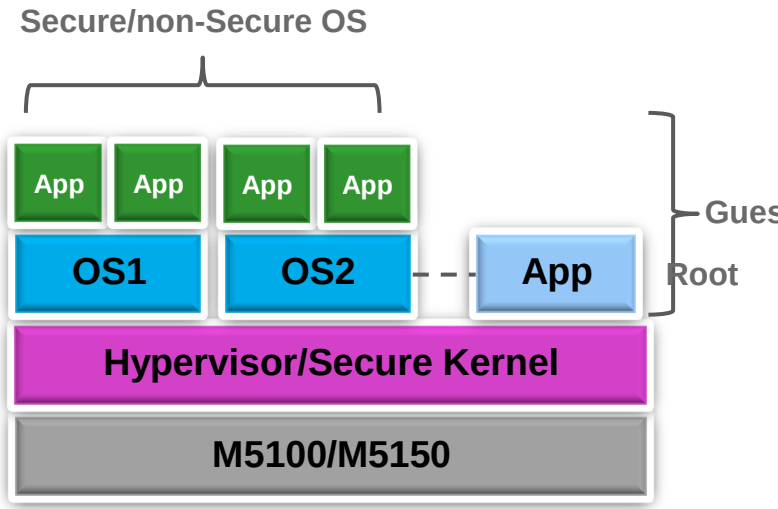
Virtualized System

- Root is the secure hypervisor
- **Multiple Guest OSes are protected**
- Guest User Apps are protected

MIPS M51xx hardware virtualization highlights

Rich set of Trusted Execution Environment features and benefits

- Secure
  - Root is the secure hypervisor/kernel
  - Guest access rights controlled by Root
- Flexible, fit for purpose
  - Full VZ using Root/Guest TLB MMU (M5150)
  - Lightweight VZ using Root/Guest FMTs (M5100)
- Scalable
  - Supports up to 7 Guests (OS and/or Apps)
- Ease of use
  - No modification required to Guest OS
  - Hypervisor software available
- High performance
  - Architected to minimize Guest-Root traffic



MIPS M51xx - Hypervisors

Open source versions available; others in development

- **Kernel Virtual Machine** 
  - Type II hypervisor.
  - Implemented as a kernel module within Linux
  - Leverages considerable amount of Linux kernel features
- **Fiasco-OC.** 
  - Type 1 L4 microkernel hypervisor
  - Virtual Machine Manager runs in Root-User context. Very secure
  - User application services and libraries provided by L4 Runtime Environment

KVM and Fiasco available for evaluation

- **Partner Hypervisors**
  - Developments in progress

MIPS M51xx – anti-tamper features

Tamper resistance for additional security

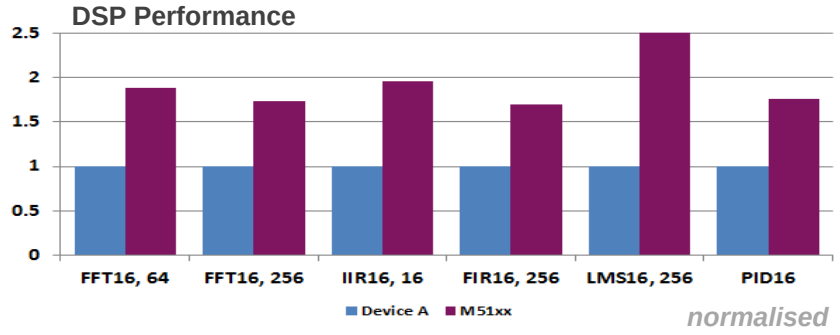
Countermeasures against unwanted access to the processor

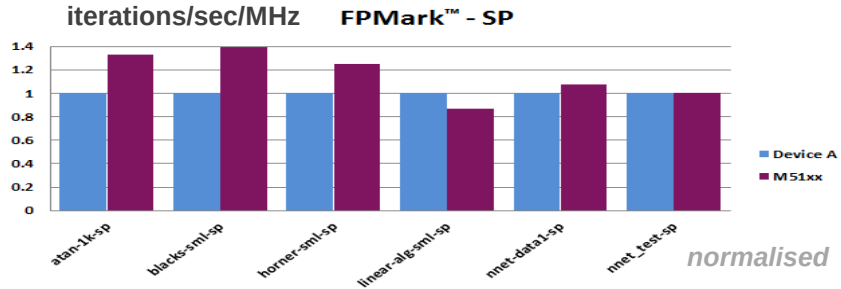
- **Hardware security**
  - User defined scrambling of $ RAM and SPRAM data/address
- **Timing and power analysis countermeasure**
  - Injection of random pipeline stalls
- **Random number sources**
  - 2 pseudo random number generators for use by user software and core logic

High performance efficiency

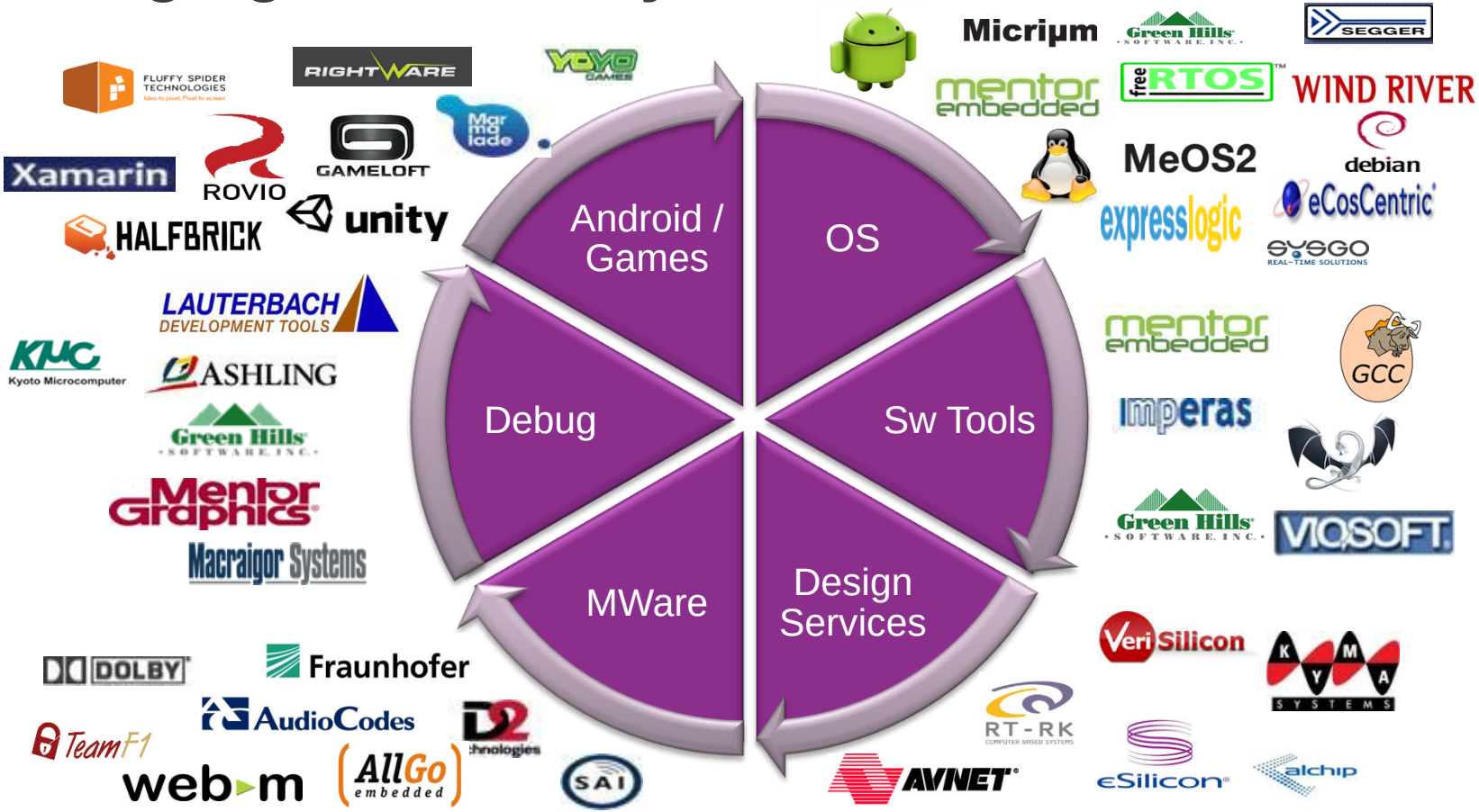
Best in Class application-specific processing

- Performance, Area, Power
  - High frequency, up to 576 MHz @ 28HPM
  - Typically, less than 20mW dynamic power, less than 0.3 mm^2 size
- Dedicated DSP & SIMD engine
  - Single cycle multiply and MAC operations
  - 2x performance of the competition
- Floating Point Unit
  - Supports single and double precision
  - Most instructions execute with 1 FPU cycle throughput and 4 cycle latency





Leveraging MIPS ecosystem



Introducing MIPS Warrior M-class cores

MIPS M51xx Cores – First MCU-class CPUs with hardware virtualization

- **Bring a new level of security and reliability to a wide range of entry-level smart embedded applications**
- **Ideal for industrial control, IoT, wearables, cloud computing, automotive, storage applications and more**
- **Continue MIPS M-class leadership in core, DSP, FPU performance and features**
- **Available in microcontroller and embedded processor versions**
- **Supported by a growing ecosystem**

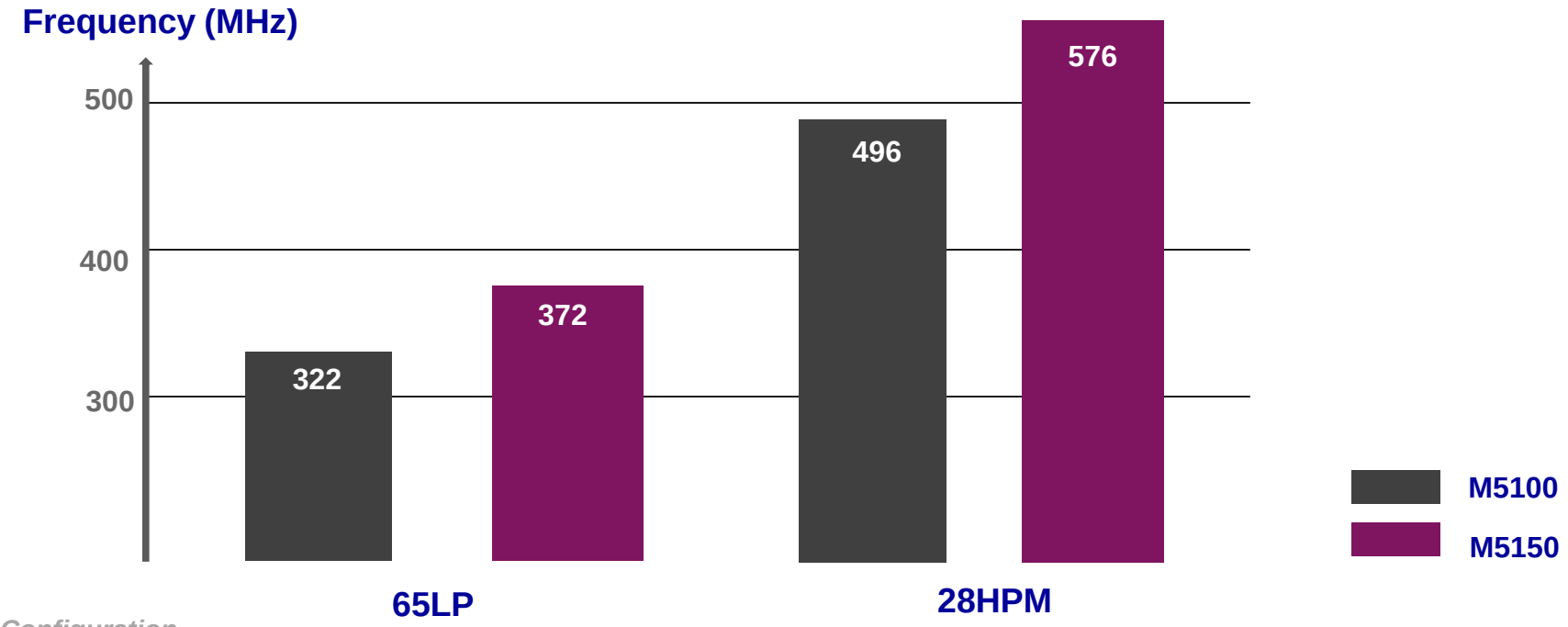
Multiple licensees. Production RTL released

Thank You!

Back Up Slides

M5100 / M5150

PPA - Frequency



Configuration
M5100: microMIPS + DSP + FPU + 32RPU + 32K/32K I/D SRAM + AHB
M5150: microMIPS + DSP + FPU + 32RTLB/32GTLB + 32K/32K $I/$D + AHB
debug not included

M5100 / M5150

Area and Power – Speed & Area Optimized

M5100	Speed		Area	
	65LP	28HPM	65LP	28HPM
Area (mm^2)*	0.77	0.23	0.2	0.04
Dynamic Power (uW/MHz)	107	39	53	17
M5150	**Speed**		**Area**	
	65LP	28HPM	65LP	28HPM
Area (mm^2)*	0.89	0.26	0.31	0.07
Dynamic Power (uW/MHz)	132	66	69	24
Std Cell Lib	9T-LVt	12T-SVt	9T SVt	9T LVt

** Core Floorplanned Area*

Configuration

M5100 speed: microMIPS + DSP + FPU + 32RPU + 32K/32K I/D SRAM

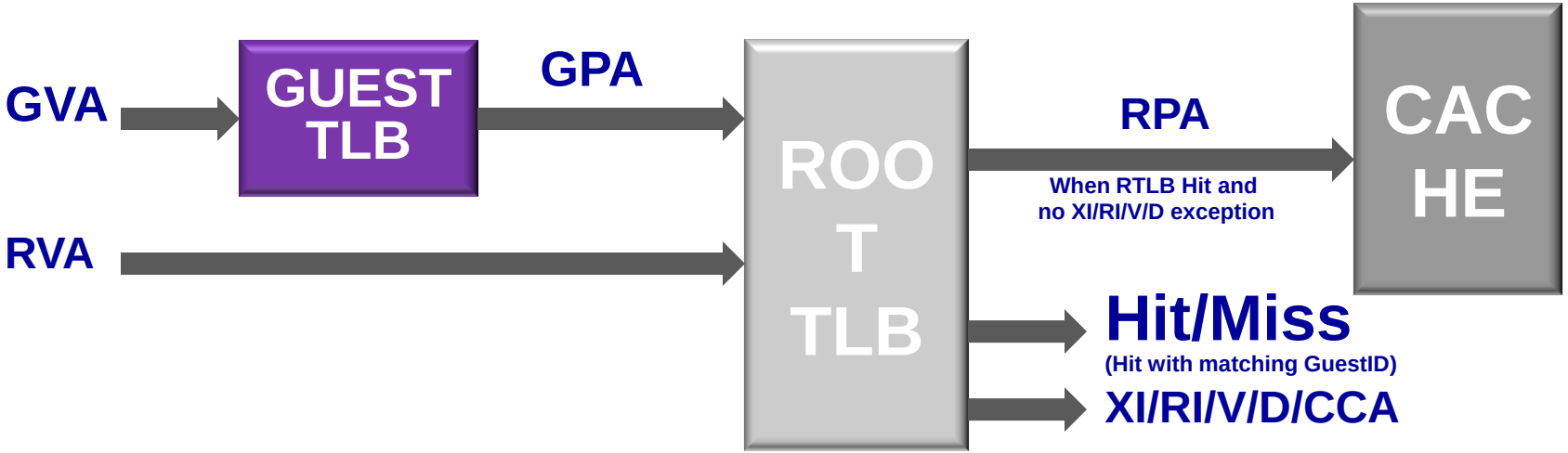
M5100 area: microMIPS + DSP + 8RPU

M5150 speed: microMIPS + DSP + FPU + 32RTLB/32GTLB + 32K/32K $I/$D

M5150 area: microMIPS + DSP + 16RTLB/16GTLB + 8K/8K $I/$D

debug not included

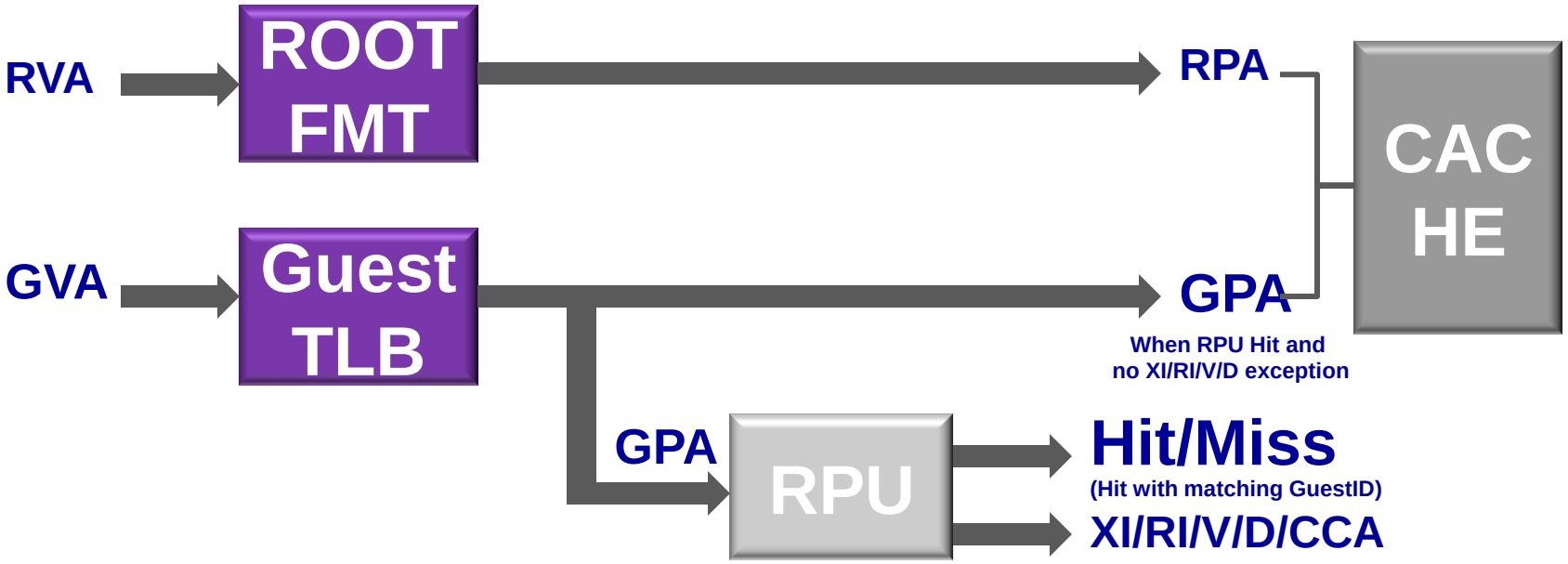
M5150 Virtualization – MMU Option 1



RVA = Root Virtual Address
RPA = Root Physical Address
GVA = Guest Virtual Address
GPA = Guest Physical Address

- XI : Execute Inhibit
- RI : Read Inhibit
- V : Valid
- D : Dirty bit
- CCA : Cacheability

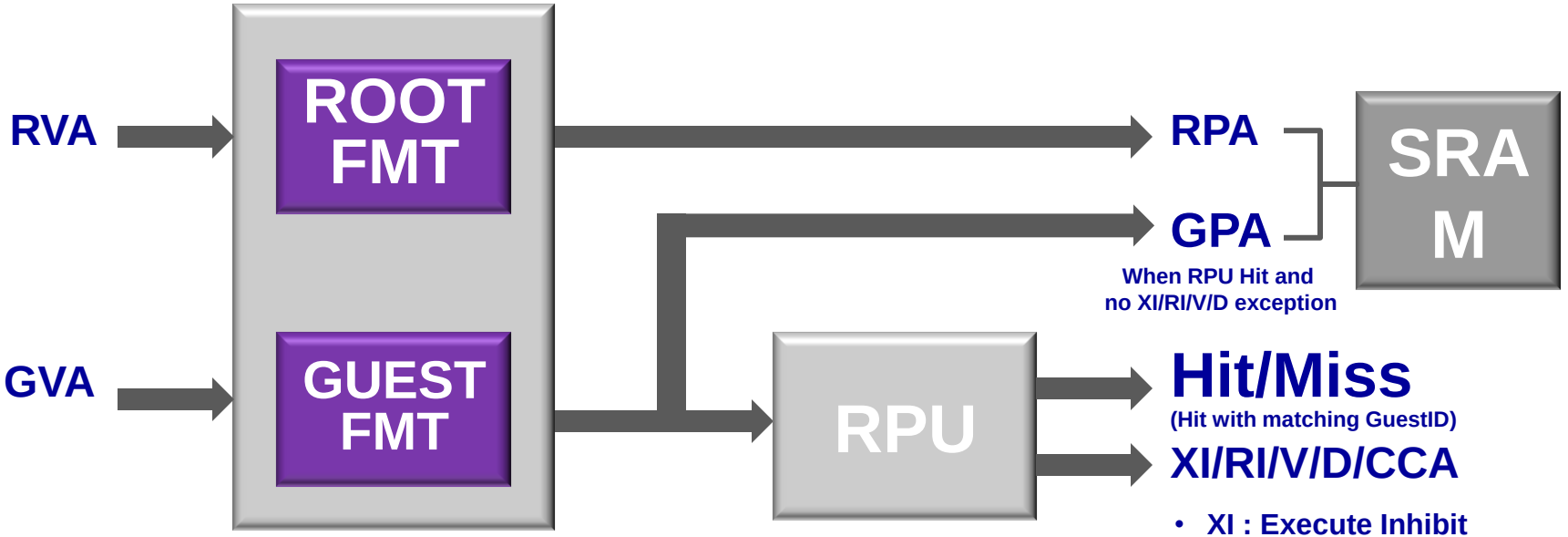
M5150 Virtualization – MMU Option 2



RVA = Root Virtual Address
RPA = Root Physical Address
GVA = Guest Virtual Address
GPA = Guest Physical Address

- XI : Execute Inhibit
- RI : Read Inhibit
- V : Valid
- D : Dirty bit
- CCA : Cacheability

M5100 Virtualization – ‘Lightweight’ version



RVA = Root Virtual Address
RPA = Root Physical Address
GVA = Guest Virtual Address
GPA = Guest Physical Address

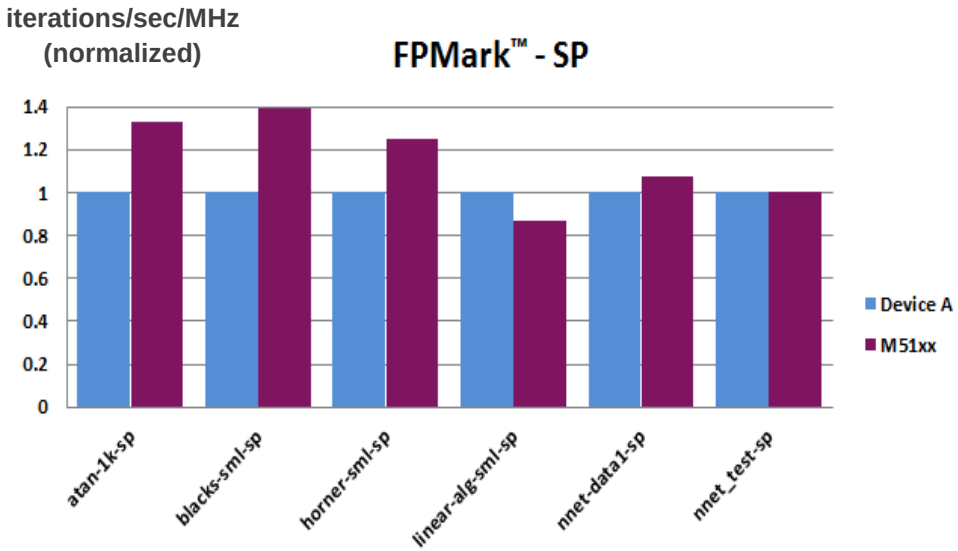
Use Case – Need for protected code

- OEM completes and packages the unfinished product:
  - Protect SoC Developer IP from OEM
  - Protect OEM IP from SoC Developer
- OEM buys 3rd Party IP to load onto the system:
  - Protect 3rd Party IP from OEM
- OEM needs to call functions in both SoC Developer and 3rd Party IP
- Requires shared memory for data

MIPS M51xx Floating Point Unit

Well-proven FPU for high performance real-time control

- Supports single and double precision datatypes. IEEE 754 compliant
- 7-stage pipeline, operates in parallel to integer pipeline
- Executes at 1:1 Core:FPU clock ratio
- Most instructions execute with 1 FPU cycle throughput and 4 cycle latency
- Support MIPS32 and microMIPS instructions

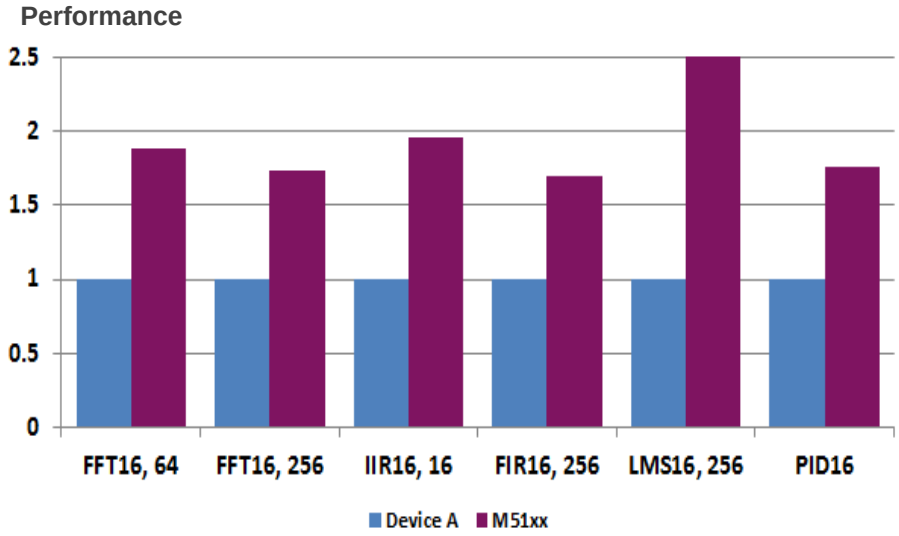


M5150: 16K/16K $I/$D

MIPS M51xx DSP

Best in class, high performance signal processing capability

- Dedicated DSP & SIMD engine
  - 150+ instructions, including 70 SIMD and 38 Multiply/MAC instructions
- Supports 8-, 16- and 32-bit integer and fractional data types
- Enhanced Multiply/Divide unit
  - Single cycle throughput multiply and MAC operations
  - Supports 32x32, 16x16, dual 16x16, dual 8x8, dual 8x16
- Supports up to 4 accumulators



Thank You!