MIPS CPUs: Differentiating the Next Wave of Innovation

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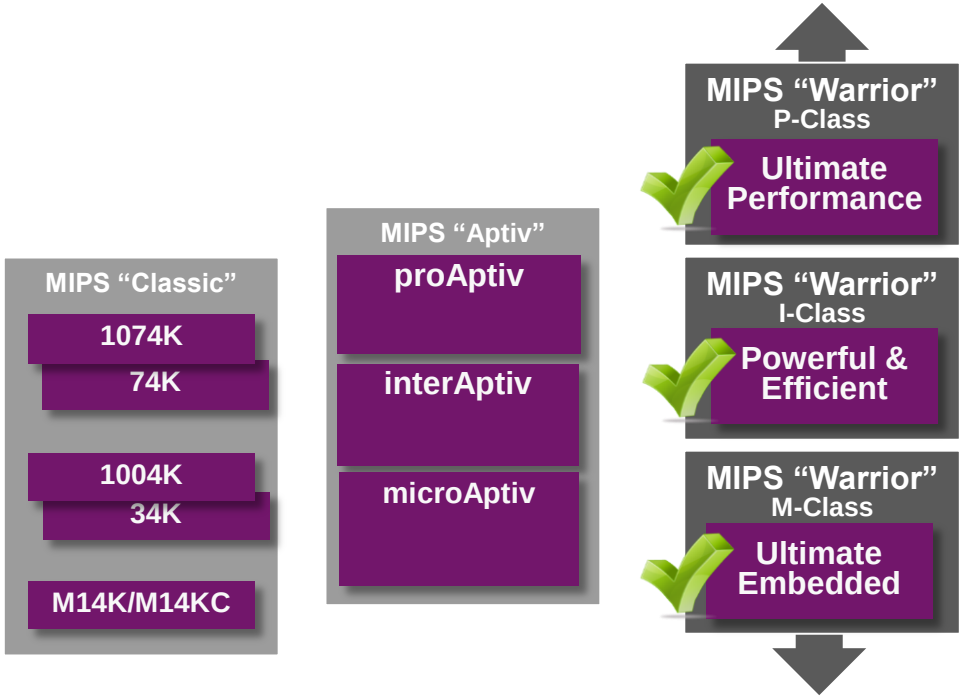
Overview

- **MIPS overview**
  - Hardware architecture better than ever
  - Software tools and OS support stronger than ever
  - Ecosystem stronger and bigger than ever
- **Leadership in embedded**
  - Bringing hardware-enforced security to embedded MCUs
- **Unique features**
  - Virtualization from high end to low end; multi-threading; advanced Power Management
- **Scaling to multicore**
  - There’s more than one way – with MIPS

MIPS IP core portfolio

A proven, efficient 64/32bit architecture - 5 generations over 30 years…

MIPS by Imagination

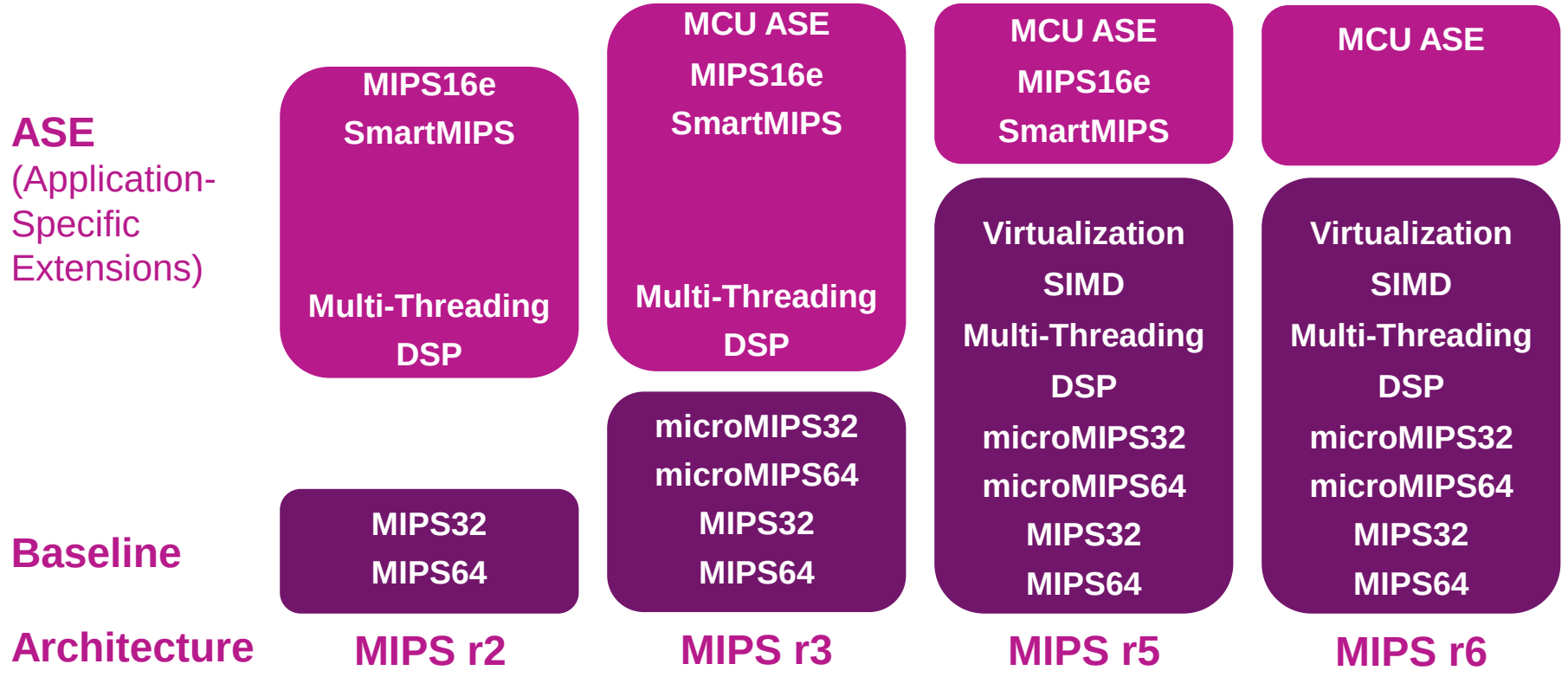


- Proven MIPS architecture
- Total compatibility 32 => 64-bit
- Hardware virtualization in all cores
- Superior multi-domain security
- Hardware multi-threading
- Compiler-aware 128-bit SIMD
- Advanced SP/DP FPU
- Consistent tool chains
- Extensive 64 & 32-bit ecosystems

MIPS Architectures

Release Updates

MIPS by Imagination



MIPS32/64 Architectures and Release 6

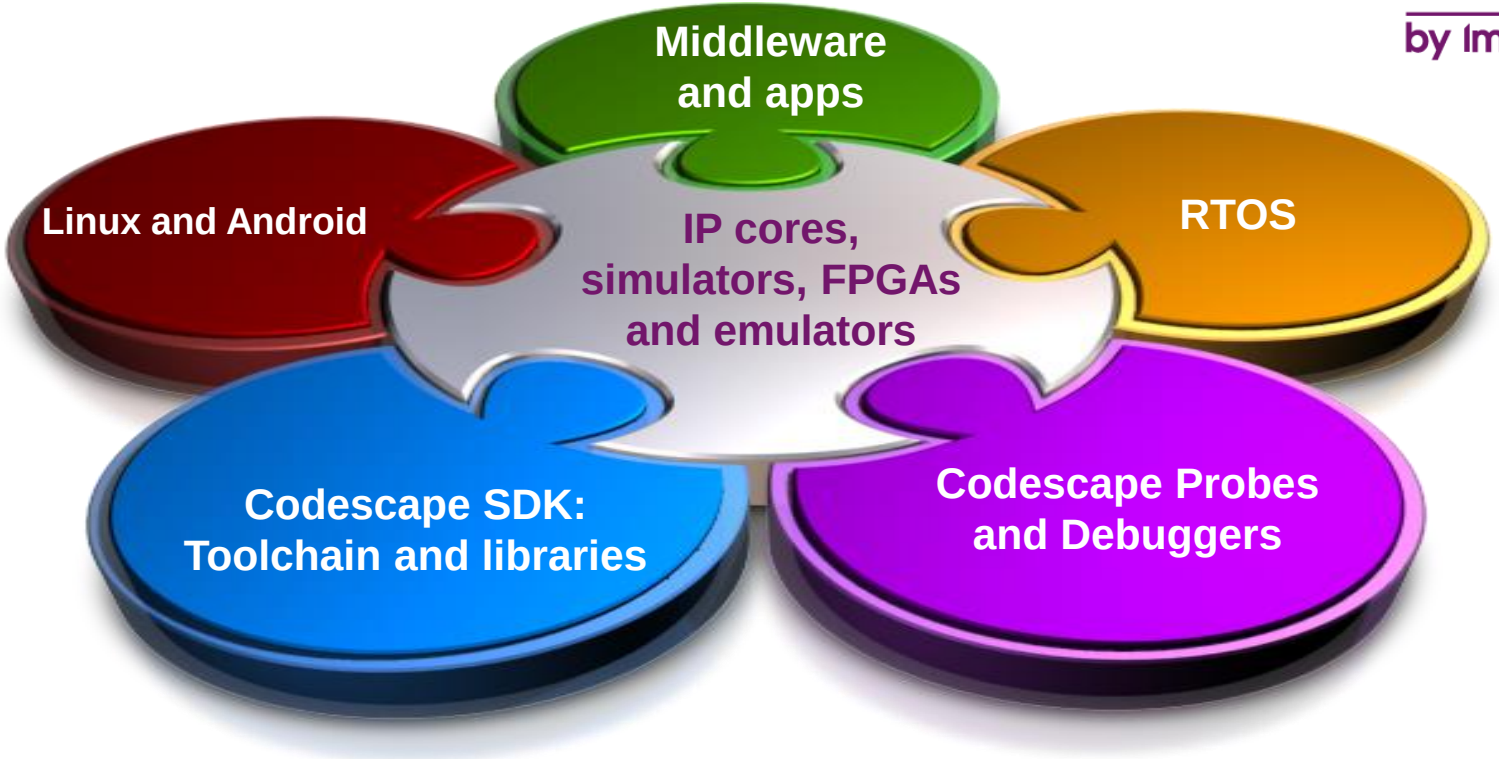
Instructions dealing with 64-bit data

- ***MIPS64***
  - Is MIPS32, plus instructions for 64-bit data types
  - Runs MIPS32 software without mode switching
- ***MIPS64/32 Release 6***
  - Streamlining a highly efficient architecture
  - Modernization of architecture through:
    - Additional instructions for enhanced execution on modern software workloads =
    - JITs, VMs, PIC, etc. commonly found in Javascript, Browsers, abstracted compiler technologies (i.e. LLVM)

MIPS: the ultimate 64/32-bit architecture

Complete portfolio of software & tools

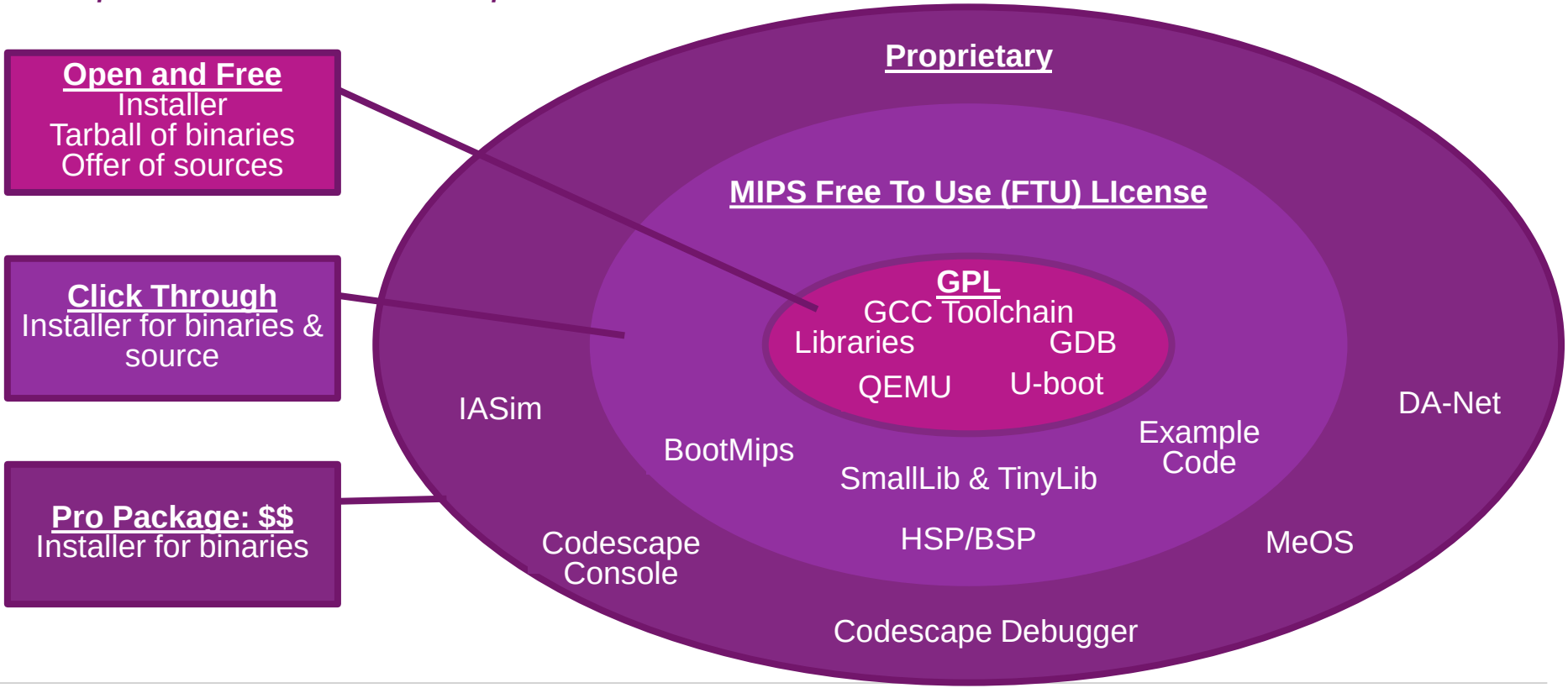
MIPS by Imagination



Comprehensive tools for every aspect of your development

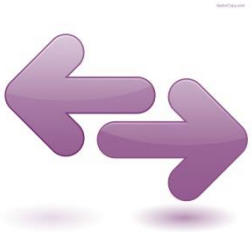
Codescape SDK integrates all the components

Complete Software Development Kit



MIPS communities are growing

prpl: at the heart of MIPS open source



Portability

To create ISA agnostic software for rapid deployment across multiple architectures

Virtualization & Security

To enable multi-tenant, secure software environments in datacenter, networking and storage, home, mobile and embedded

Heterogeneous Computing

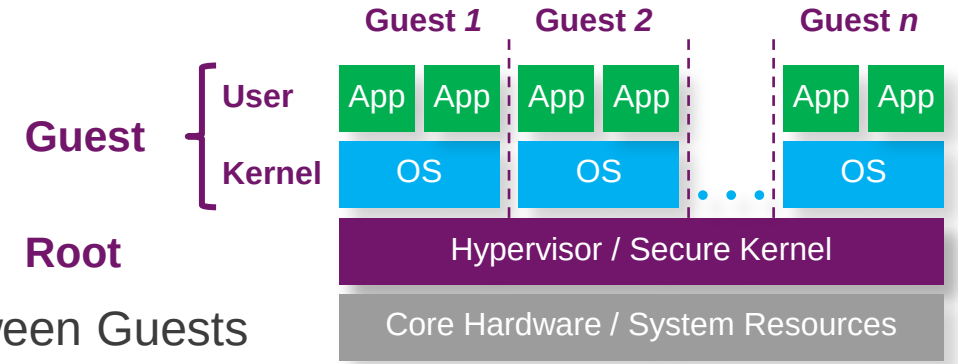
To leverage heterogeneous architectures and compute resources enabling efficient processing for applications such as big data analytics

www.prplfoundation.org

OmniShield and MIPS

HW Virtualization is the foundation

- **Virtualization is a SW concept – what CPU HW enhances support?**
  - A new privilege level (***Root***) in the architecture:
  - Supporting multiple guest domains

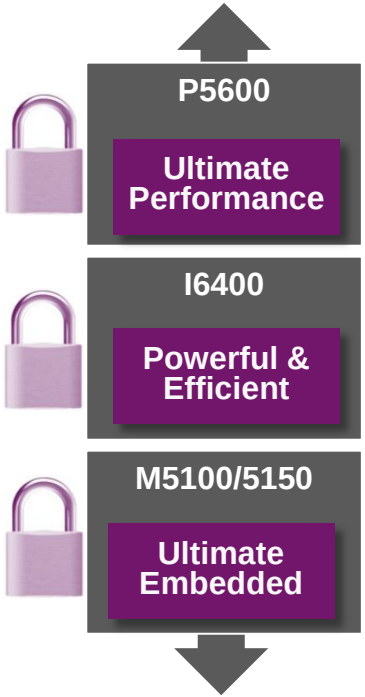


  - Minimizing context switch costs between Guests
    - New CP0 registers for management, control and extended functionality for Guests
    - New instructions for Root-privilege Read/Write/Invalidate of Guest resources
      - CP0 context, TLB
    - Extension of TLB/MMU resources for Guest/Root assignment

HW virtualization top to bottom core lineup

Only MIPS implements Virtualization for Embedded MCUs!

MIPS by Imagination



- 16-stage SuperScalar (SS) Out-of-Order (OoO) Multi-core CPU
- Up to 15 guests

- 9-stage SuperScalar (SS) Multi-Threaded Multi-core CPU
- Up to 31 guests

- 5-stage MCU and embedded MPU cores
- Up to 7 guests

OmniShield by Imagination

Virtualization & HW multi-threading

Unique features making MIPS the better choice

MIPS by Imagination

- **GPR Shadow Register Sets (SRSs) – replication(s) of primary GPR set**
  - Supported in M-class M5100/M5150 with hardware VZ, up to 16 SRSs
  - Enables low latency, fast context switch for high priority interrupts and exception handling
  - Real time response - works across guest domains, preserving low latency and deterministic response without hypervisor intervention

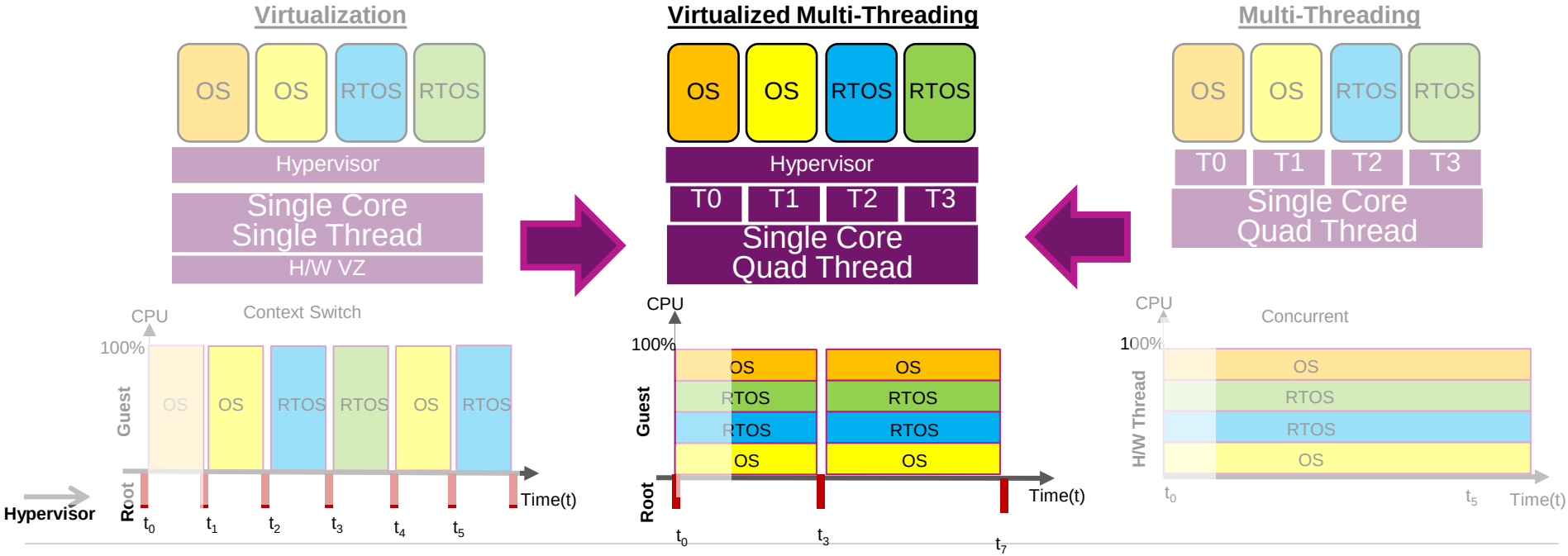
- **Hardware Multi-Threading – replicate(s) full CPU context, plus scheduling**
  - Supported in I-class I6400 with hardware VZ, up to 4 threads (Virtual Processors) per core
  - Enables Guests <-> VPs assignment – secures execution of each thread
  - Guest domain execution can switch on a clock cycle by cycle basis, and…
  - Each superscalar I6400 core can run code for multiple Guests simultaneously per cycle

Virtualization and HW multi-threading in action

Intersection of isolation and concurrency

Concurrent multi-domain execution environment

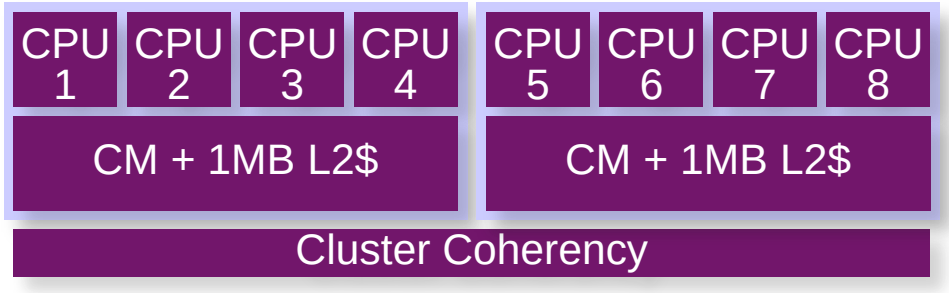
zero overhead + real-time response



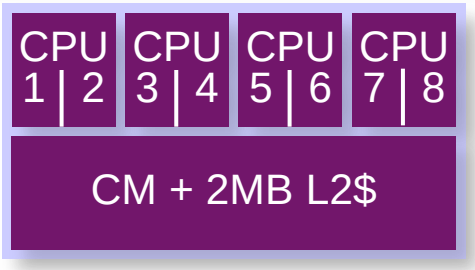
Scaling multicore to 8 (& more)

Useful processor performance

- **Are 8 cores useful for AP function?**
  - Questionable, at best…
  - But it has become a marketing feature



- **What if the cost for 8 CPUs could be reduced?**
  - Traditional approach: Dual quad core clusters
  - Alternative: Use HW Multi-Threading to reduce the number of cores
    - Quad core cluster with 2 threads/core = 8 CPUs
    - 4 Cores = plenty of real app performance
    - Configs shown have 2MB or 1MB of L2$



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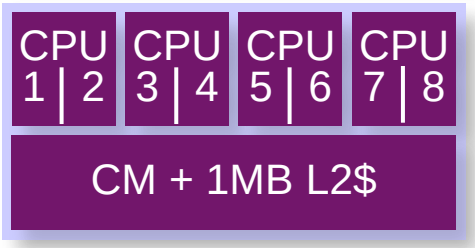
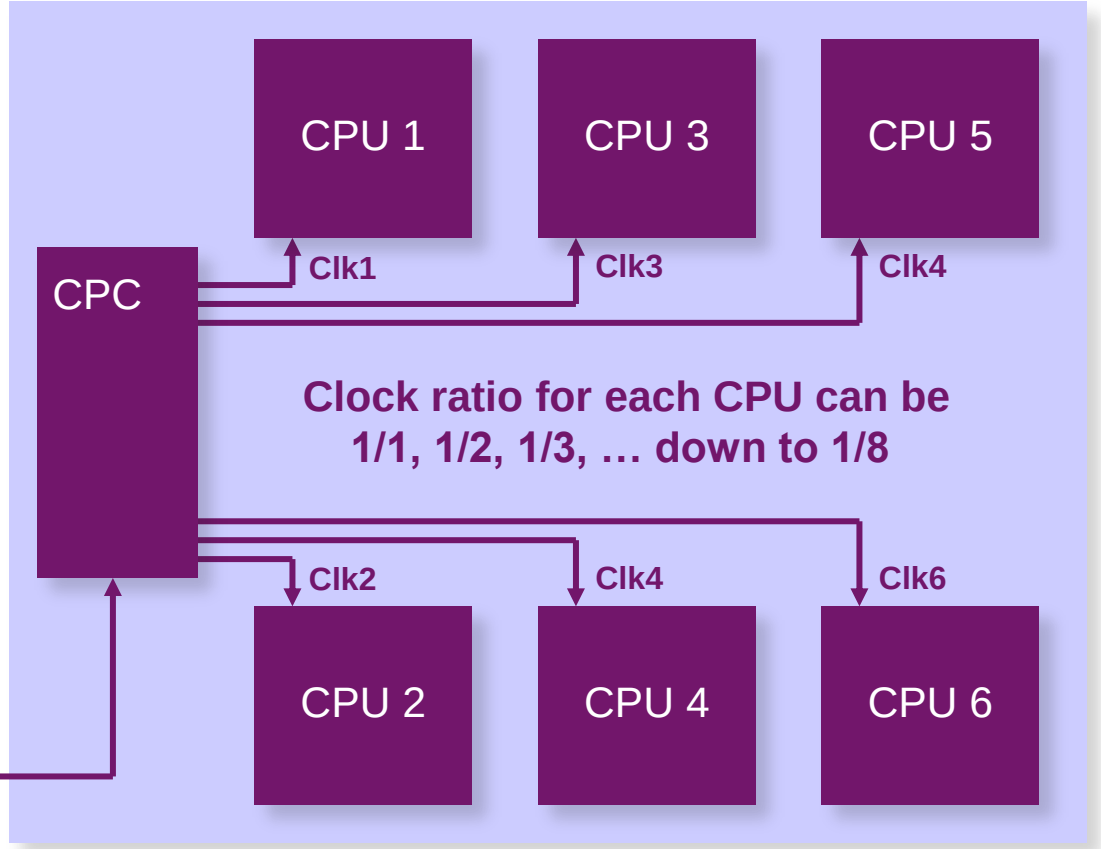


~ 1/2 the size

Advanced Power Management

Dynamic Clocking Per CPU

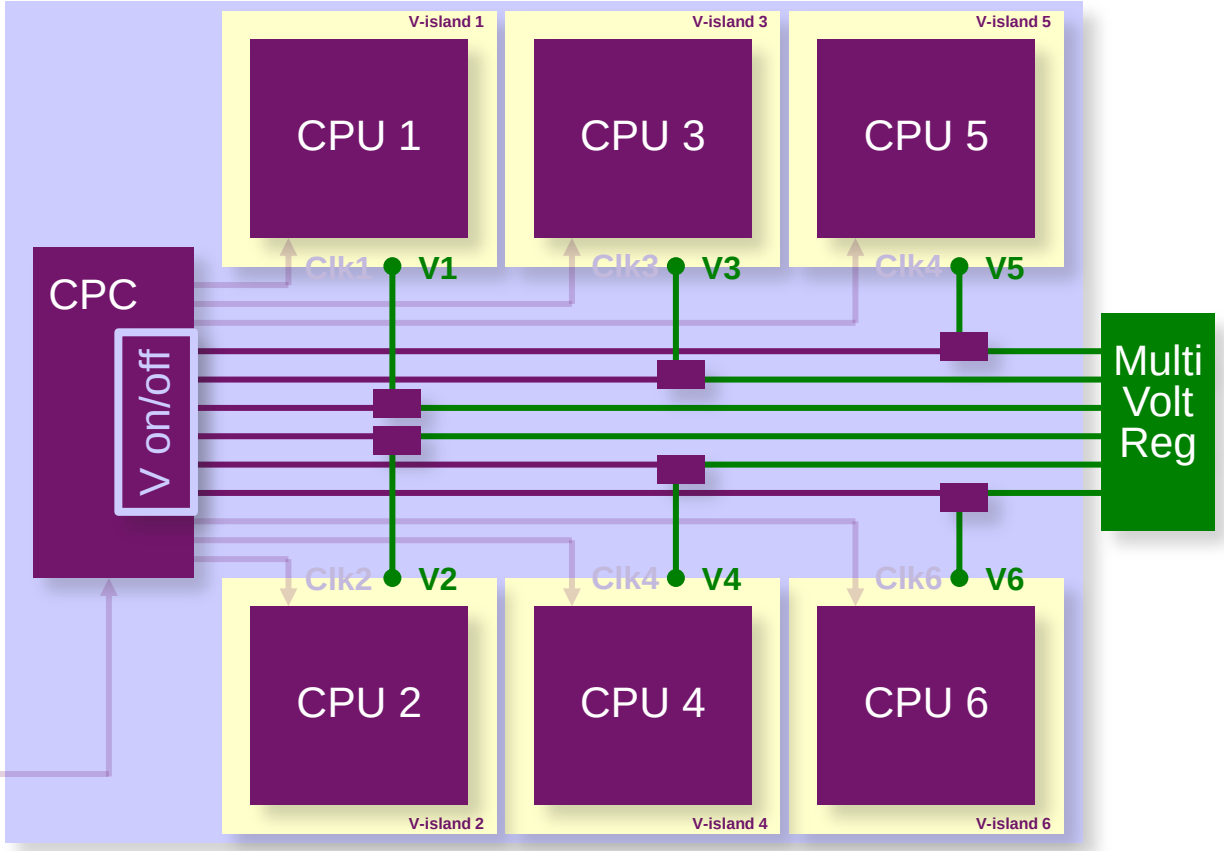
- **One Main clock to CPC**
- **CPC clk output, per CPU**
  - On/Off
  - Integer ratios of main clock
  - Dynamic/run time control
- **Tuned performance to workloads**



Advanced Power Management

Dynamic Voltage Per CPU

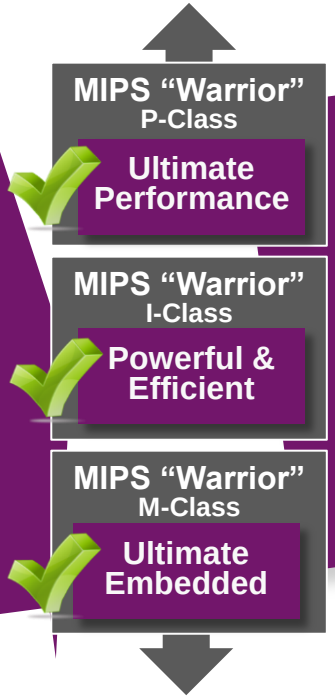
- **Power island per CPU**
- **External multi-output voltage regulator**
- **CPC provides per CPU**
  - On/Off voltage gating
  - Dynamic/run time control
- **Optimizes to minimal power per workload**



Building the future

MIPS by Imagination

- >6B MIPS CPUs shipped
- Volumes growing for past 5 years
- Compelling SPEC & CoreMark performance and PPA specs
- 64-bit CPUs shipping in significant and growing volume



- Class leadership for all CPU families
- Efficient heterogeneous solutions for phones, tablets, STBs, networking, IoT
- High reliability and scalable security
- Streamlined architecture optimized for new generations of processing

Thank you!

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